

BOXER-6313U

Fanless Embedded Vehicle Box PC

User's Manual 2nd Ed

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Packing List

Before setting up your product, please make sure the following items have been shipped:

Item	Quantity
● BOXER-6313U	1
● GPS antenna	1
● Screw pack	1
● Phoenix 3-pin DC-in power connector	1
● Phoenix 2-pin Remove Power Switch connector	1
● Product DVD with User's Manual (in pdf) and drivers	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device
19. **DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.**

FCC Statement

Warning!



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.

China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
印刷电路板 及其电子组件	○	○	○	○	○	○
外部信号 连接器及线材	○	○	○	○	○	○
外壳	○	○	○	○	○	○
中央处理器 与内存	○	○	○	○	○	○
硬盘	○	○	○	○	○	○
电源	○	○	○	○	○	○

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注:

一、此产品所标示之环保使用期限, 系指在一般正常使用状况下。

二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products
 AAEON Embedded Box PC/ Industrial System

Component	Poisonous or Hazardous Substances or Elements					
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	○	○	○	○	○	○
Wires & Connectors for External Connections	○	○	○	○	○	○
Chassis	○	○	○	○	○	○
CPU & RAM	○	○	○	○	○	○
Hard Disk	○	○	○	○	○	○
PSU	○	○	○	○	○	○

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

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Chapter 1

Product Specifications

1.1 Specifications

System

- **Processor** Intel® Atom™ E3845 1.91 GHz Processor
- **System Memory** 204 pins DDR3L 1333MHz SODIMM x 1, up to 8 GB
- **Display Interface** DB-15 x 1 for VGA
HDMI x 1
- **Storage** 2.5" SATA HDD bay x 2 (optional mSATA)
- **Front I/O Panel**
 - DB-15 x 1 for VGA
 - HDMI x 1
 - Power switch (w/ LED) x 1
 - 2-pin remote reset switch connector x 1
 - Antenna holes x 4 (GPS x 1 Wi-Fi x 1, 2G/ 3G/ 4G x 3)
 - CAN Bus x 2 (Raw and open CAN supported)
 - Front access lockable 2.5" SATA HDD bay x 2
 - System power LED x 1 (Green)
 - HDD active LED x 1 (Red)
 - Power status LED (Green)
- **Rear I/O Panel**
 - USB 3.0 x 1
 - USB 2.0 x 3
 - 10/100/1000 Mbps GbE RJ-45 x 2
 - Full size MiniCard connector x 3 (one support USB only, optional mSATA)
 - RS-232 x 2
 - RS-232/422/485 x 2 (Select with BIOS)
 - Line-out x 1

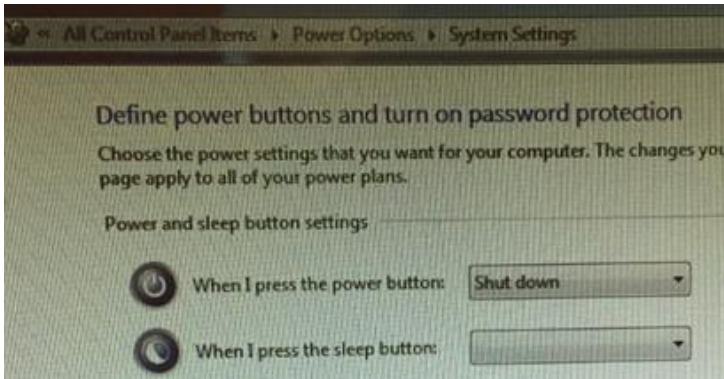
- **Expansion Slot**
 - Mic-in x 1
 - 3-pin terminal block power input x 1
 - Full size MiniCard slot x 3
 - SIM slot x 3
- **OS Support**
 - Windows® 8.1 32/64-bit
 - Windows® 7 32/64-bit
 - Windows® Embedded Standard 7 32/64-bit
 - Windows® Embedded Standard 8 32/64-bit
 - Linux
- **Power**
 - DC 12 V or 24 V w/ 3-pin terminal block

Mechanical

- **Operating Temperature**
 - 15 ~ 60°C (-5°F ~ 140°F) with 0.5m/s Airflow, E3845 processor, Wide Temp. DRAM & Wide Temp. HDD. MiniCard not included
- **Storage Temperature**
 - 40 ~ 80°C (-40 ~ 176°F)
- **Storage Humidity**
 - 5~90% @40°C, non-condensing
- **Anti-Vibration**
 - 1 Grms / 5~ 500Hz / operation – Automotive HDD
- **Anti-Shock**
 - 15G peak acceleration (11 msec. duration) –HDD
- **EMC**
 - CE /FCC class A
- **Vehicle Certification**
 - ISO-7636
 - E-13

1.2 Note for Windows® 7 Users

For Windows® 7 users, please set the power button from “Do Nothing” to “Shut down” when pressed to prevent problems during shut down or other errors (such as the Windows Error Recovery error message).



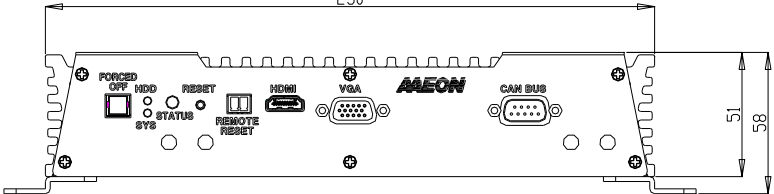
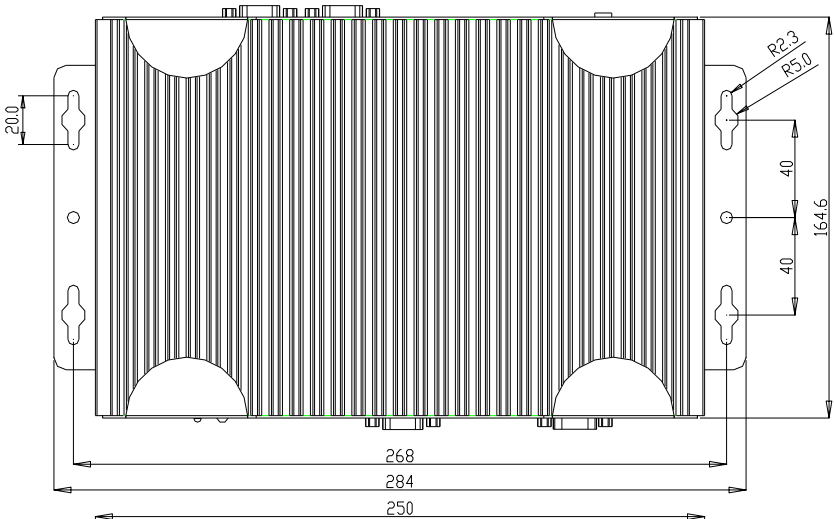
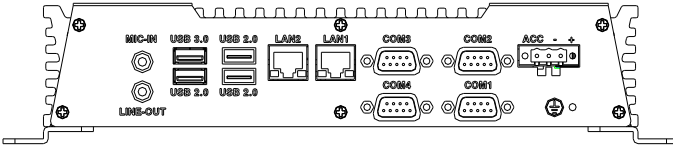
To perform this change, please follow the steps below:

- 1) Go to Control Panel
- 2) Open Power Options and select “Change what the power buttons do” option
- 3) Select “Shut down” from the drop-down list for the power buttons
- 4) Save changes and exit

Chapter 2

Hardware Information

2.1 Dimensions

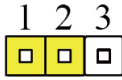


2.2 List of Jumpers

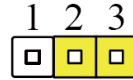
Please refer to the table below for all of the system's jumpers that you can configure for your application

Label	Function
JP2	Clear CMOS
JP9	COM3 +5V/+12V RING selection
JP10	COM2 +5V/+12V RING selection

2.2.1 Clear CMOS (JP2)



Normal (Default)



Clear CMOS

2.2.2 COM3 +12V/+5V/Ring Selection (JP9)

Pin	Signal
1-2	+12 V
3-4	Ring (Default)
5-6	+5 V

2.2.3 COM3 +12V/+5V/Ring Selection (JP10)

Pin	Signal
1-2	+12 V
3-4	Ring (Default)
5-6	+5 V

2.3 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

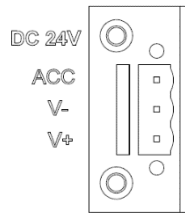
Label	Function
CN1	RTC connector
CN5	Display Port connector
CN13	SATA power connector (+5V/12V)
CN15	MiniCard 1 connector w/ onboard SIM (Full size MiniCard)
CN16	SIM 1 socket
CN17	MiniCard 2 connector w/ onboard SIM (Full size MiniCard)
CN18	SIM 2 socket
CN19	MiniCard 3 connector w/ onboard SIM (Full size MiniCard)
CN20	SIM 3 socket
CN21	Dual stack USB connector (2.0/3.0)
CN22	Dual stack USB connector (2.0)
CN24	Remote switch connector
CN26	5-wire touch connector
CN30	SPI connector
CN37	LAN1 connector
CN38	LAN2 connector
CN39	DC-in
CN45	External DC power in Connector
CN53	SATA Port1 connector
CN54	SATA Port2 connector
CN60	MCU Delay ON/OFF/Voltage Select
CN62	HDMI connector
CN63A	COM1 connector

CN63B	COM2 connector
CN64A	COM4 connector
CN64B	COM3 connector
CN66	SATA Power connector (+5V/12V/G-Sensor)
CN69	VGA connector
DIMM1	DDR DIMM slot
SW1	HW reset connector

2.3.1 SATA power connector (+5V/12V) (CN13)

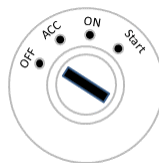
Pin	Signal
1	+12 V
2	GND
3	GND
4	+5 V

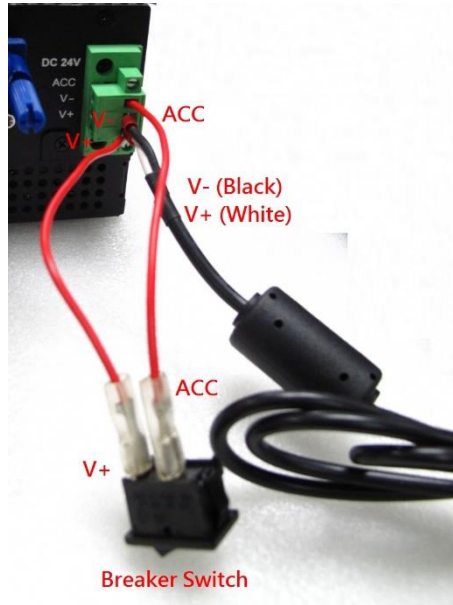
2.3.2 DC-Inlet (DC in)



Pin	Label	Definition
1	V+	V+ for DC power
2	V-	V- for DC power
3	ACC	Accessories (Ignition)

*ACC is one of the selectable positions on a car ignition switch (illustrated below). ACC is a short form for “accessories,” and turning the key to this position enables electronic devices, such as the radio and air-conditioner, to be powered by the vehicle’s battery (DC current).





Since the voltage requirement for ACC is usually the same as voltage of the battery, users may connect V+ to ACC to power up the BOXER-6301VS, or disconnect it to power off the machine.

Because the ACC signal control acts on a PSON signal and can therefore generate a smooth/clean shutdown of the OS (Windows/Linux), the system supports only ATX mode.

The "Delay on/off" functions can be configured by setting up the bootup/shutdown timer. Users may refer to section 2.38 for details.

2.3.3 MiniCard 1 connector (Full size) w/ onboard SIM (CN15)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		

6	+1.5V	PWR	+1.5V
7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	

35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

2.3.4 MiniCard 2 connector (Full size) w/ onboard SIM (CN17)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V

7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	PCIE_RX-	DIFF	
24	+3.3VSB	PWR	+3.3V
25	PCIE_RX+	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	PCIE_TX-	DIFF	
32	SMB_DATA	I/O	+3.3V
33	PCIE_TX+	DIFF	
34	GND	GND	

35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

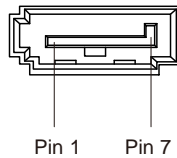
2.3.5 MiniCard 3 connector (Full size) w/ onboard SIM (CN19)

Pin	Pin Name	Signal Type	Signal Level
1	PCIE_WAKE#	IN	
2	+3.3VSB	PWR	+3.3V
3	NC		
4	GND	GND	
5	NC		
6	+1.5V	PWR	+1.5V

7	PCIE_CLK_REQ#	IN	
8	NC	PWR	
9	GND	GND	
10	NC	I/O	
11	PCIE_REF_CLK-	DIFF	
12	NC	IN	
13	PCIE_REF_CLK+	DIFF	
14	NC		
15	GND	GND	
16	NC	PWR	
17	NC		
18	GND	GND	
19	NC		
20	W_DISABLE#	OUT	+3.3V
21	GND	GND	
22	PCIE_RST#	OUT	+3.3V
23	M-SATA_RXP	DIFF	
24	+3.3VSB	PWR	+3.3V
25	M-SATA_RXN	DIFF	
26	GND	GND	
27	GND	GND	
28	+1.5V	PWR	+1.5V
29	GND	GND	
30	SMB_CLK	I/O	+3.3V
31	M-SATA_TXN	DIFF	
32	SMB_DATA	I/O	+3.3V
33	M-SATA_TXP	DIFF	
34	GND	GND	

35	GND	GND	
36	USB_D-	DIFF	
37	GND	GND	
38	USB_D+	DIFF	
39	+3.3VSB	PWR	+3.3V
40	GND	GND	
41	+3.3VSB	PWR	+3.3V
42	NC		
43	GND	GND	
44	NC		
45	NC		
46	NC		
47	NC		
48	+1.5V	PWR	+1.5V
49	NC		
50	GND	GND	
51	NC		
52	+3.3VSB	PWR	+3.3V

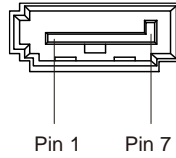
2.3.6 SATA Port 1 Connector (CN53)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	

4	GND	GND
5	SATA_RX-	DIFF
6	SATA_RX+	DIFF
7	GND	GND

2.3.7 SATA Port 2 Connector (CN54)



Pin	Pin Name	Signal Type	Signal Level
1	GND	GND	
2	SATA_TX+	DIFF	
3	SATA_TX-	DIFF	
4	GND	GND	
5	SATA_RX-	DIFF	
6	SATA_RX+	DIFF	
7	GND	GND	

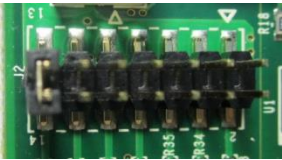
2.3.8 Input Voltage Selection (CN60)

The BOXER-6313U has special vehicle Power Supply Unit (PSU) that can provide the following power management for vehicular applications.

- Over voltage protection
- Under voltage protection
- Reverse protection
- Load dump protection
- Programmable ACC power on/off delay time

Setting DC input mode

DC Input Mode Options

Location CN60	CN60 PIN13 and pin14	Mode	Operating Voltage	Start Voltage (Refer to the note below)
	OPEN	12V	9V~18V	11V +/- 0.2V
	SHORT	24V	18V~36V	22V +/- 0.4V

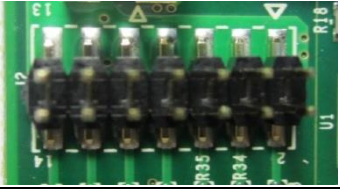
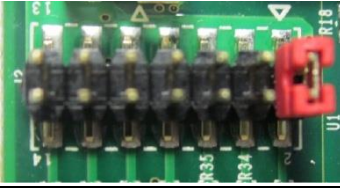
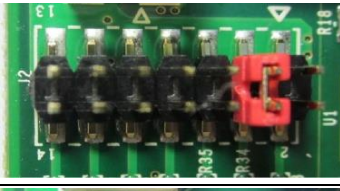
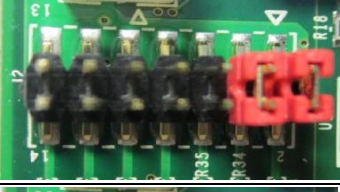
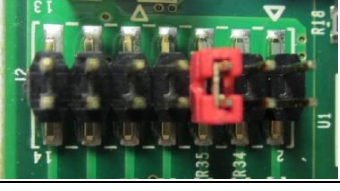
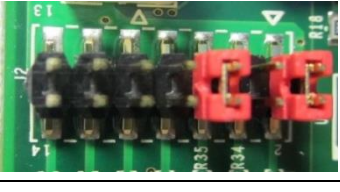
Note:

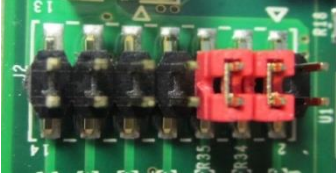
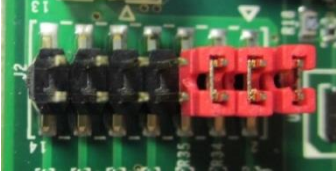
Usually, the voltage of a car battery stays at 13.5 ~15V (@ 12V Mode), or at 27 ~30V (@ 24V Mode) while the engine is running. Thus, the voltage of the battery can provide enough energy to prevent a cold crank from starting a car engine when it is higher than 11V (@ 12V Mode) or 22V (@ 24V Mode).

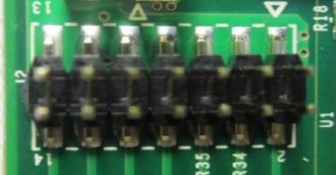
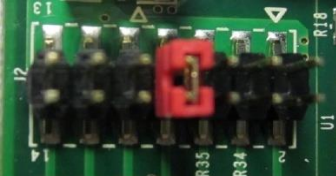
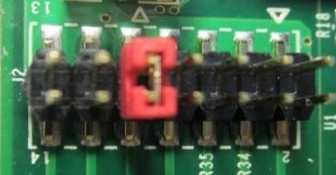
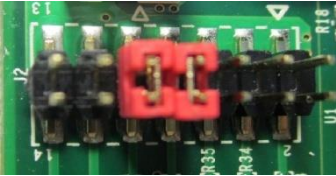
A cold crank will cause the voltage of the battery to drop to 6V (@ 12V mode) or lower, making it difficult to maintain a stable +12V power output to the BOXER-6313U and causing it to cold boot.

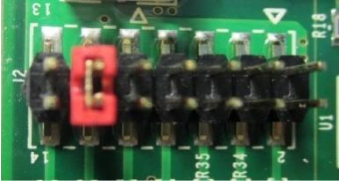
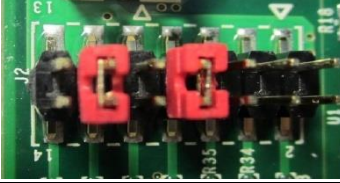
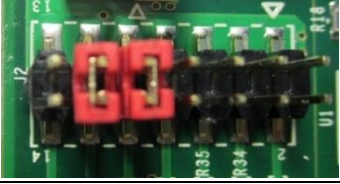
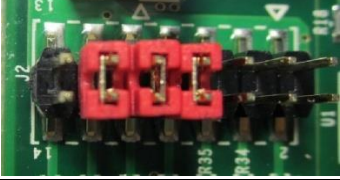
For the Initial Start Voltage, the input voltage will offer over 11V (@12V mode) or 22V (@ 24V mode) to the PSU. The PSU will operate at 9 ~18V (@12V mode) or 18 ~36V (@24V mode) after the ACC ON.

2.3.9 Delay ON/OFF/Voltage Selection (CN60)

Function	Location	Pin	Set Time
ACC Delay On		1, 2, 3, 4, 5, 6 opened	1 sec
		1, 2 shorted	3 sec
		3, 4 shorted	5 sec
		1, 2, 3, 4 shorted	10 sec
		5, 6 shorted	15 sec
		1, 2, 5, 6 shorted	20 sec

	3, 4, 5, 6 shorted	25 sec
	1, 2, 3, 4, 5, 6 shorted	30 sec

Function	Location	Pin	Set Time	
ACC Delay	Off		7, 8, 9, 10, 11, 12 opened	1 min
			7, 8 shorted	3 min
			9, 10 shorted	5 min
			7, 8, 9, 10 shorted	10 min

	11, 12 shorted	30 min
	7, 8, 11, 12 shorted	60 min
	9, 10, 11, 12 shorted	120 min
	7, 8, 9, 10, 11, 12 shorted	0 min

2.3.10 COM1 Connector (CN63A)

RS-232			
Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

2.3.11 COM2 Connector (CN63B)

RS-232			
Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

RS-422			
Pin	Signal	Pin	Signal
1	TXD-	2	TXD+
3	RXD+	4	RXD-
5	GND	6	N/C
7	N/C	8	N/C
9	N/C		

RS-485			
Pin	Signal	Pin	Signal
1	D-	2	D+
3	N/C	4	N/C
5	GND	6	N/C
7	N/C	8	N/C
9	N/C		

2.3.12 COM4 Connector (CN64A)

RS-232			
Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

2.3.13 COM3 Connector (CN64B)

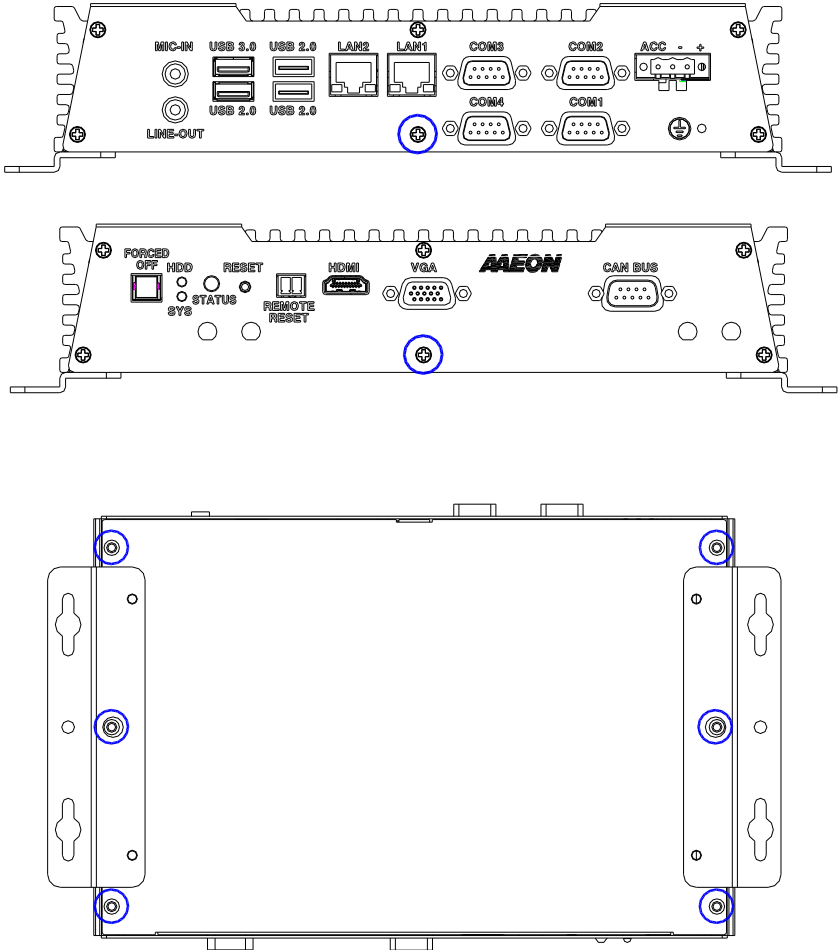
RS-232			
Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

RS-422			
Pin	Signal	Pin	Signal
1	TXD-	2	TXD+
3	RXD+	4	RXD-
5	GND	6	N/C
7	N/C	8	N/C
9	N/C		

RS-485			
Pin	Signal	Pin	Signal
1	D-	2	D+
3	N/C	4	N/C
5	GND	6	N/C
7	N/C	8	N/C
9	N/C		

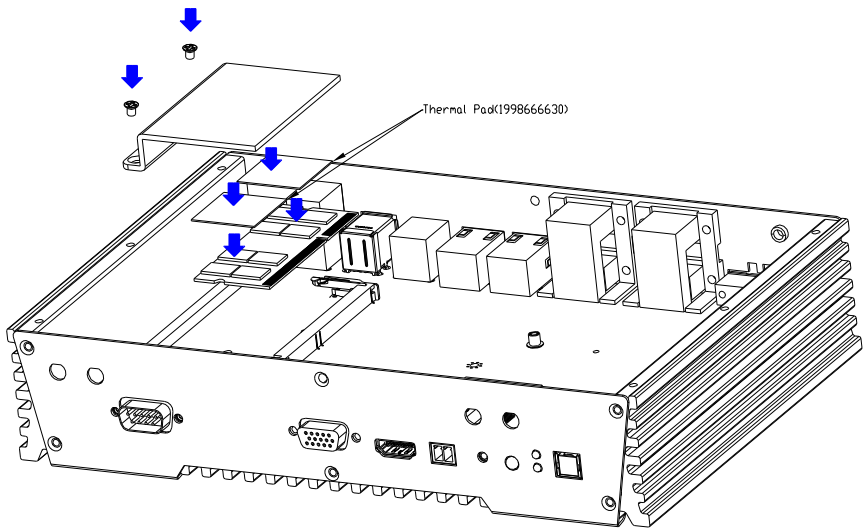
2.4 Installing RAM and MiniCard

To install RAM and MiniCard, remove the highlighted screws to access the system's interior.



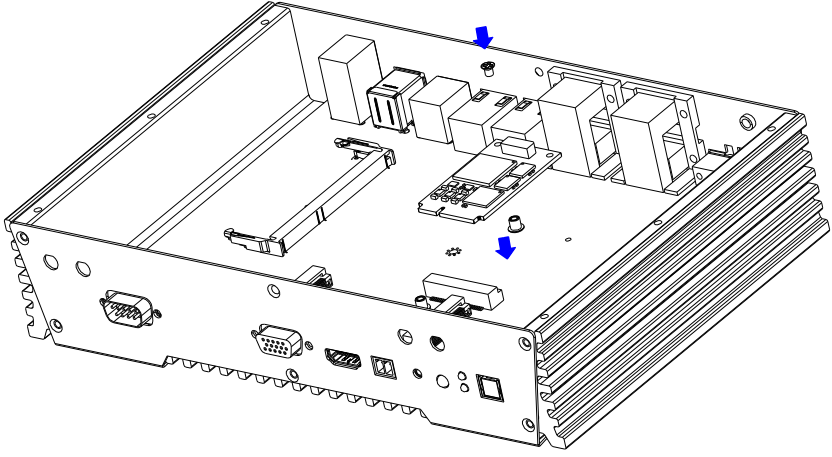
Installing RAM

To install RAM, remove the RAM cover and slot in the RAM to the RAM slot. After that, place two thermal pads (part number 1998666630) on the RAM and secure the cover.



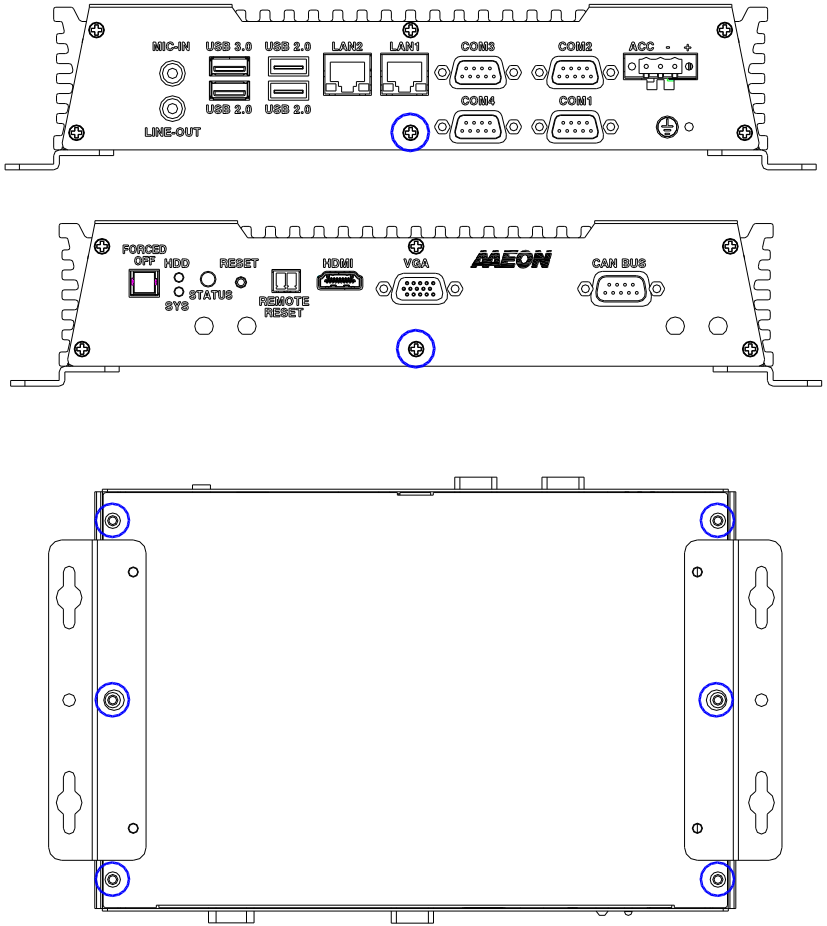
Installing MiniCard

To install MiniCard, simply slot the MiniCard into the card slot and secure with screws.

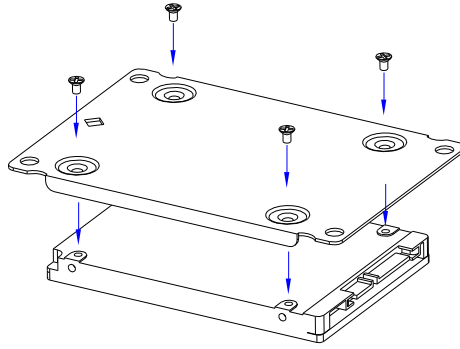


2.5 Installing HDD

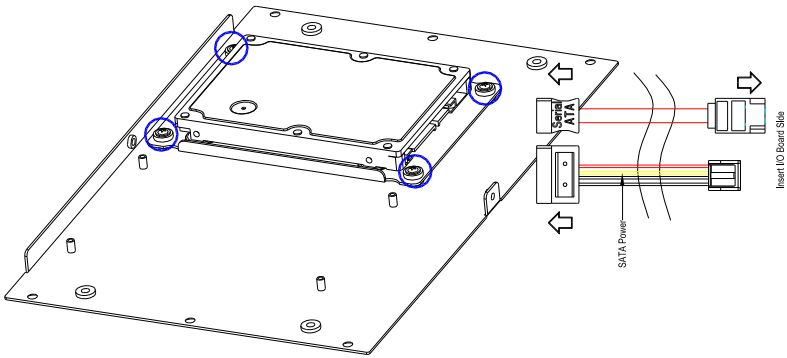
To install HDD, remove the highlighted screws to access the system's interior.



Secure the HDD onto the pad with screws.



Secure the pad onto the cover with screws and connect the cables to the connectors on the board.



Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main – Date and time can be set here. Press <Tab> to switch between date elements

Advanced – Enable/ Disable boot option for legacy network devices

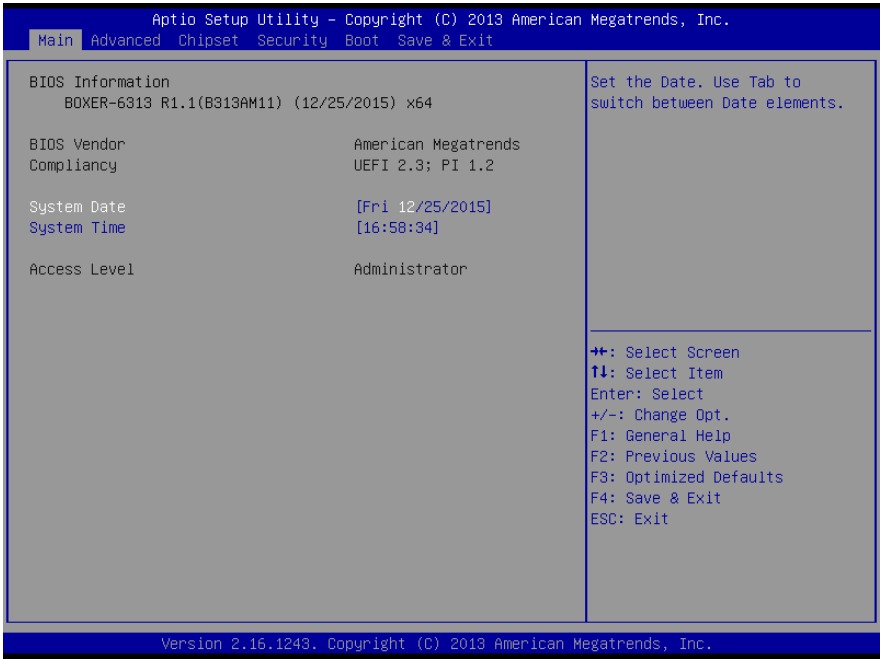
Chipset – For hosting bridge parameters

Boot – Enable/ Disable quiet Boot Option

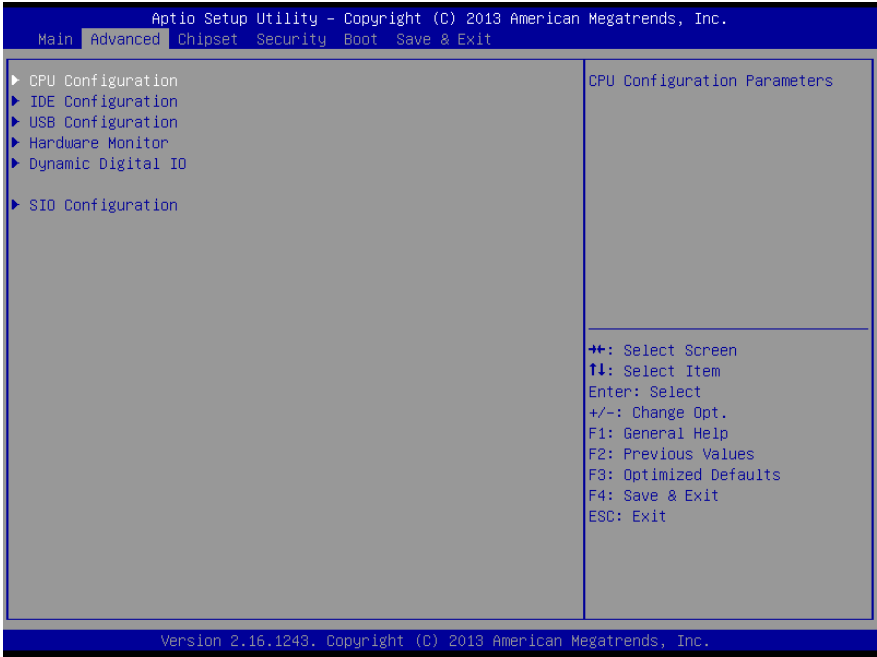
Security – The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main



3.4 Setup Submenu: Advanced



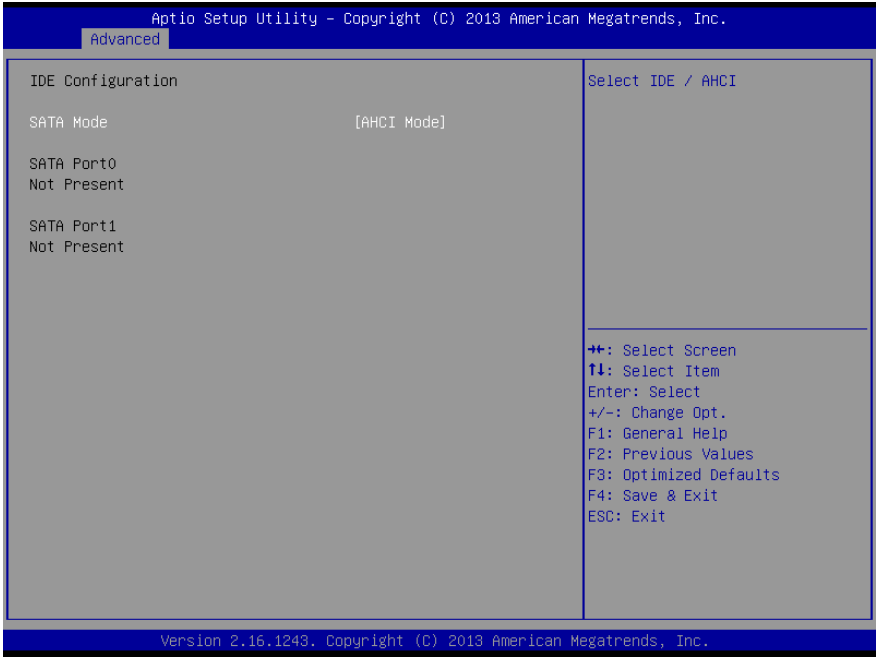
3.4.1 Advanced: SATA Configuration



Options summary:

Intel Virtualization Technology	Disabled	
	Enabled	Optimal Default, Failsafe Default
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.		
EIST	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable/Disable Intel SpeedStep		

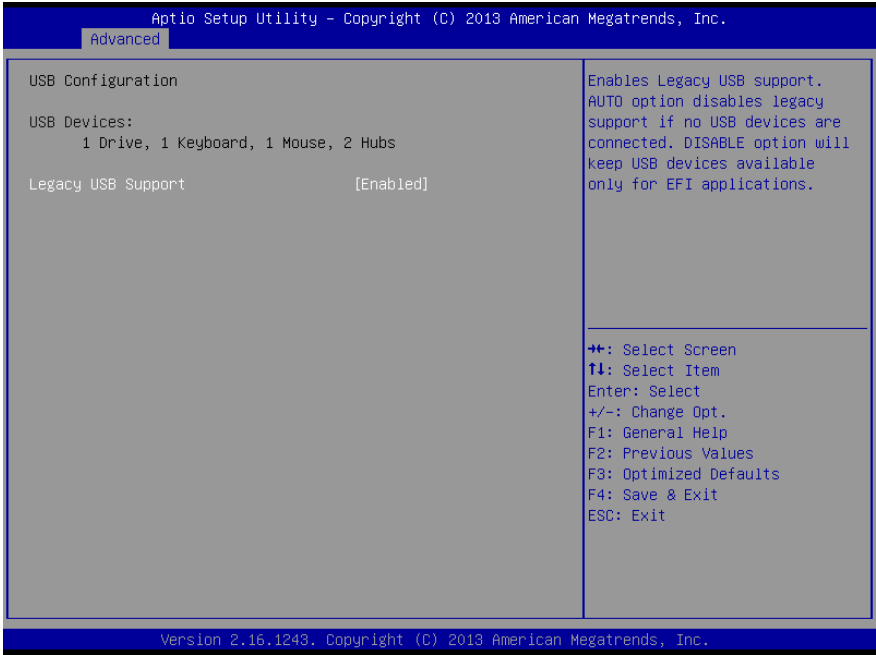
3.4.2 Advanced: IDE Configuration (IDE)



Options summary:

SATA Mode	IDE Mode	
	AHCI Mode	Optimal Default, Failsafe Default
Select IDE / AHCI		

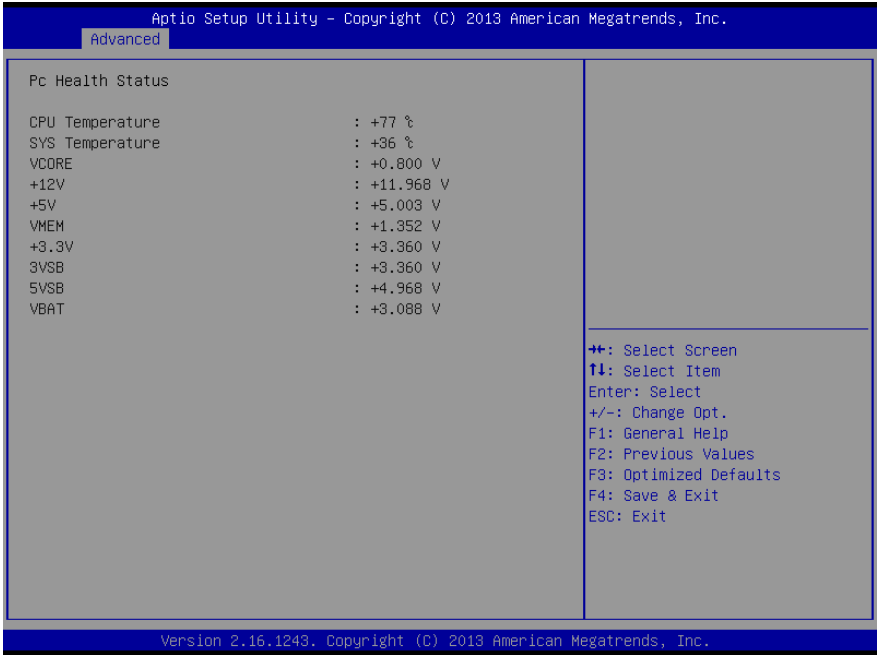
3.4.3 Advanced: USB Configuration



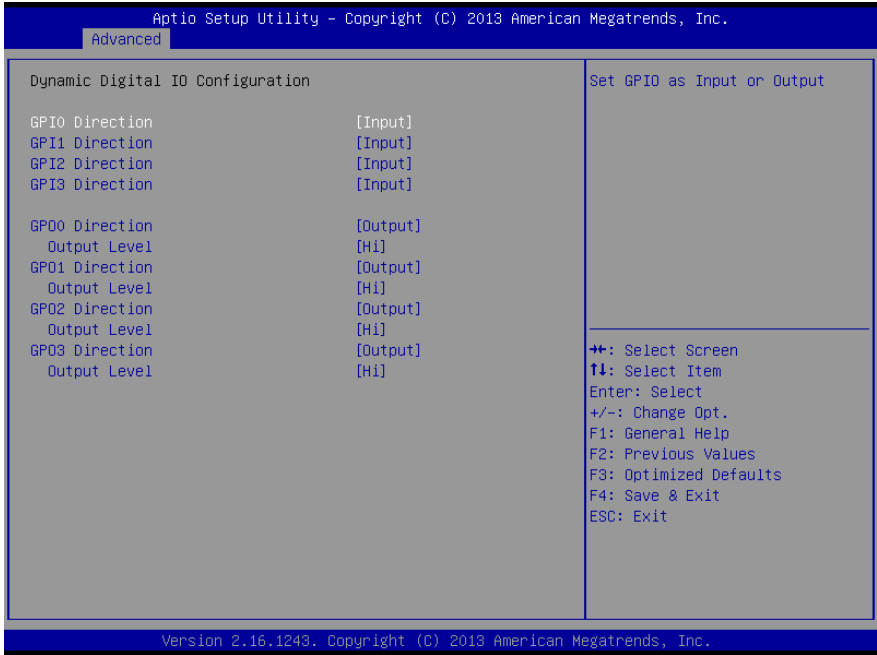
Options summary:

Legacy USB Support	Enabled	Optimal Default, Failsafe Default
	Disabled	
	Auto	
<p>Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS. AUTO option disables legacy support if no USB devices are connected</p>		

3.4.4 Advanced: Hardware Monitor



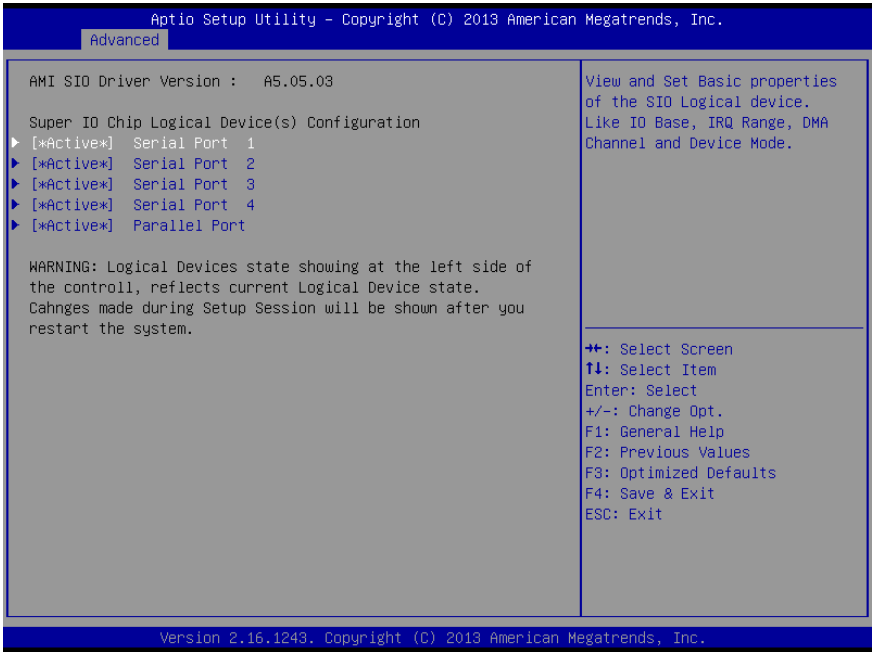
3.4.5 Advanced: Dynamic Digital IO Configuration



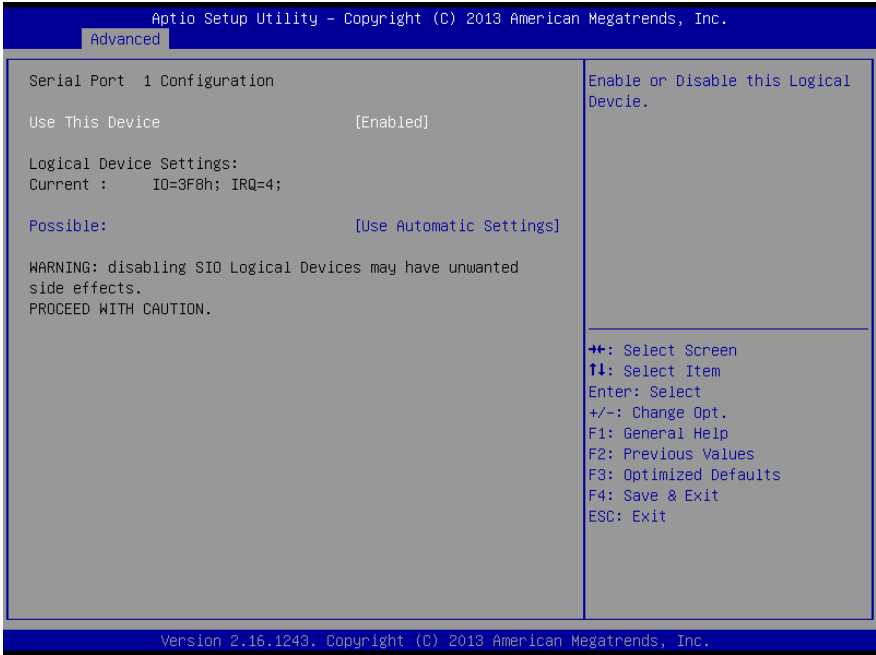
Options summary:

GPI[3:0] Direction	Input	Optimal Default, Failsafe Default
	Output	
Set GPIO as Input or Output		
GPI[3:0] Output Level	Hi	Optimal Default, Failsafe Default
	Low	
Set GPI[3:0] Output as Hi or Low		
GPO[3:0] Direction	Input	Optimal Default, Failsafe Default
	Output	
Set GPIO as Input or Output		
GPO[3:0] Output Level	Hi	Optimal Default, Failsafe Default
	Low	
Set GPO[3:0] Output as Hi or Low		

3.4.6 Advanced: SIO Configuration



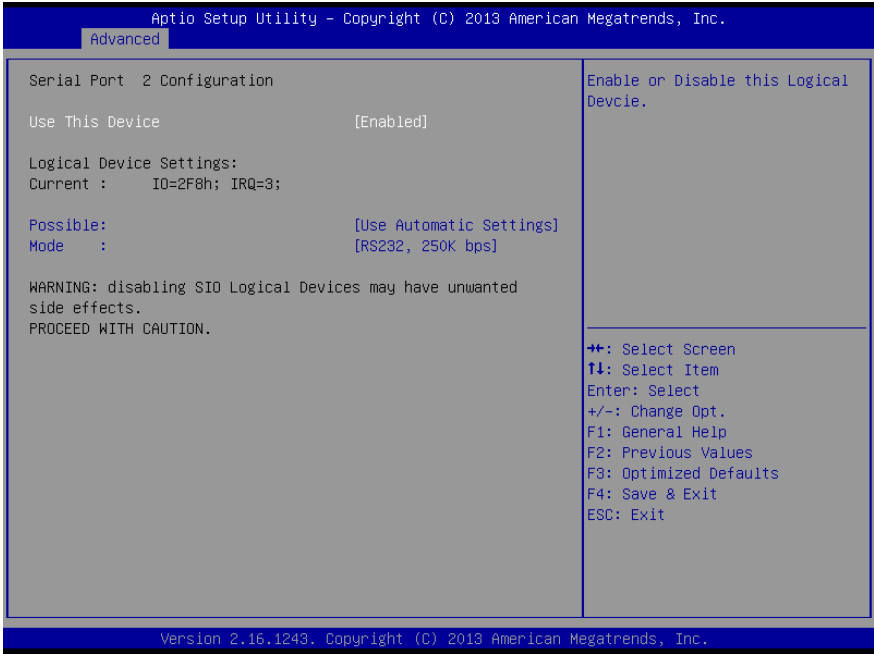
3.4.6.1 SIO Configuration: Serial Port 1 Configuration



Options summary:

Use This Device	Disabled	Optimal Default, Failsafe Default
	Enabled	
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8; IRQ=4;	
	IO=2F8; IRQ=3;	
Select an optimal setting for IO device		

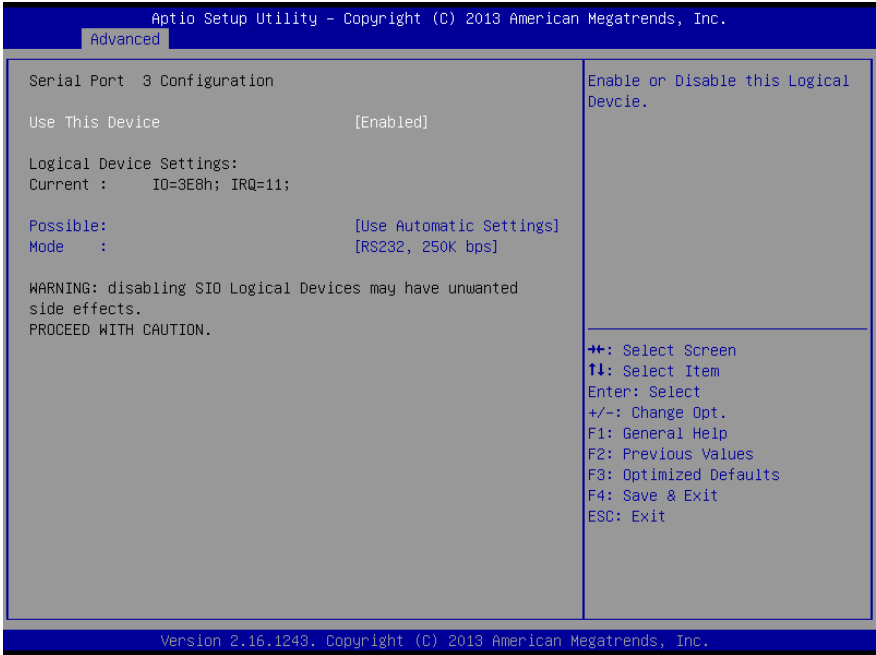
3.4.6.2 SIO Configuration: Serial Port 2 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2F8; IRQ=3;	
	IO=3F8; IRQ=4;	
Select an optimal setting for IO device		
Mode	RS232, 250K bps	Optimal Default, Failsafe Default
	RS422, 250K bps	
	RS485, Driver Half Duplex, 250K bps	
	RS485, Receiver Half Duplex, 250K bps	
	Shut Down Mode	
UART RS232, 422, 485 selection		

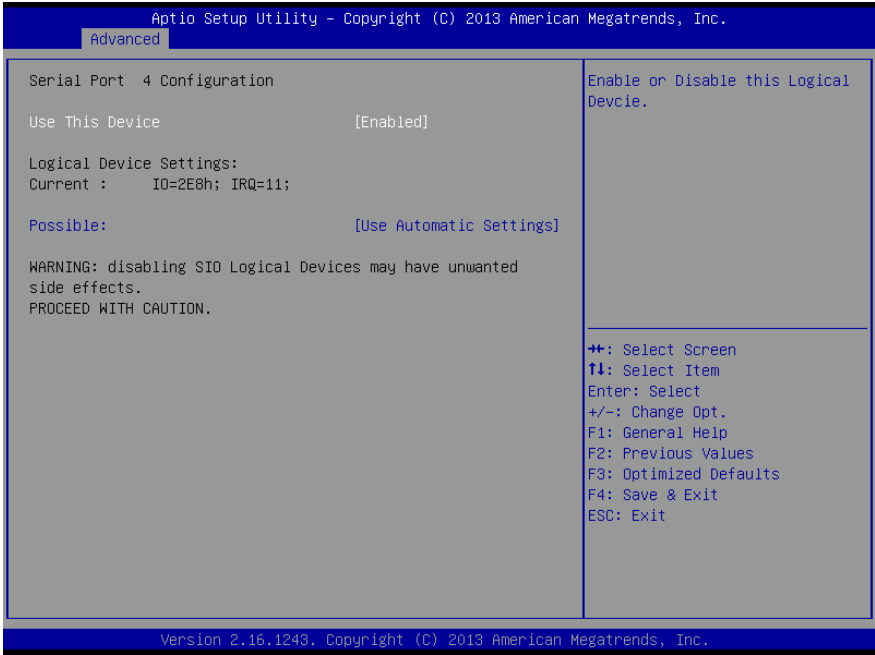
3.4.6.3 S IO Configuration: Serial Port 3 Configuration



Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3E8; IRQ=11;	
	IO=2E8; IRQ=11;	
Select an optimal setting for IO device		
Mode	RS232, 250K bps	Optimal Default, Failsafe Default
	RS422, 250K bps	
	RS485, Driver Half Duplex, 250K bps	
	RS485, Receiver Half Duplex, 250K bps	
	Shut Down Mode	
UART RS232, 422, 485 selection		

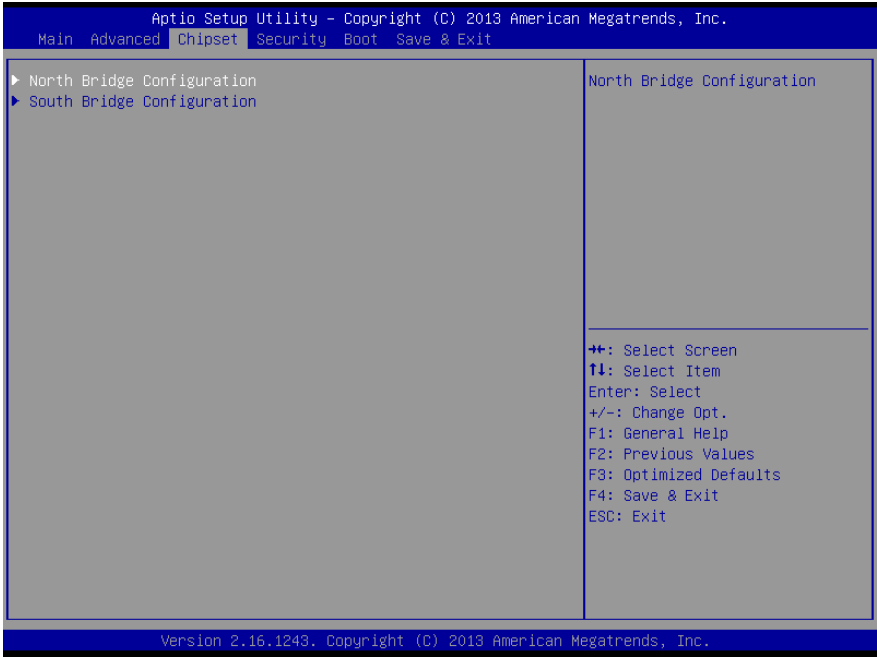
3.4.6.4 S IO Configuration: Serial Port 4 Configuration



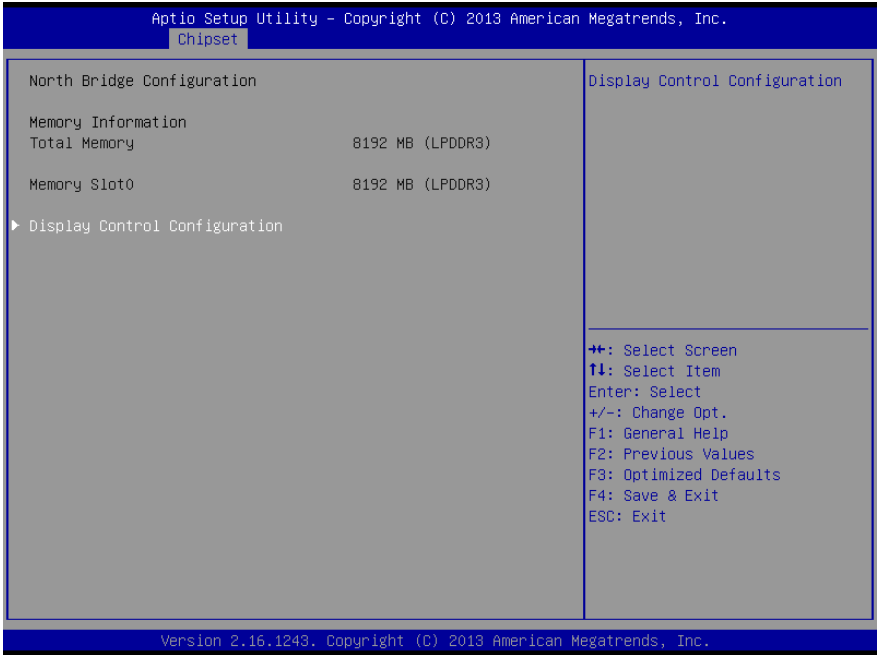
Options summary:

Use This Device	Disabled	
	Enabled	Optimal Default, Failsafe Default
En/Disable Serial Port (COM)		
Possible:	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=2E8; IRQ=11;	
	IO=3E8; IRQ=11;	
Select an optimal setting for IO device		

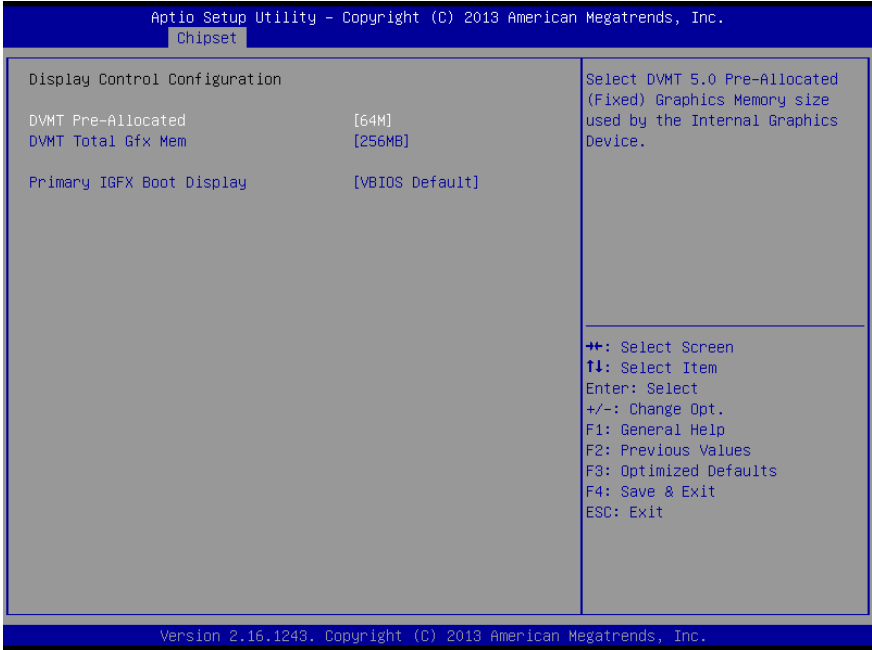
3.5 Setup submenu: Chipset



3.5.1 Chipset: North Bridge



3.5.1.1 North Bridge: Display Control Configuration



Options summary:

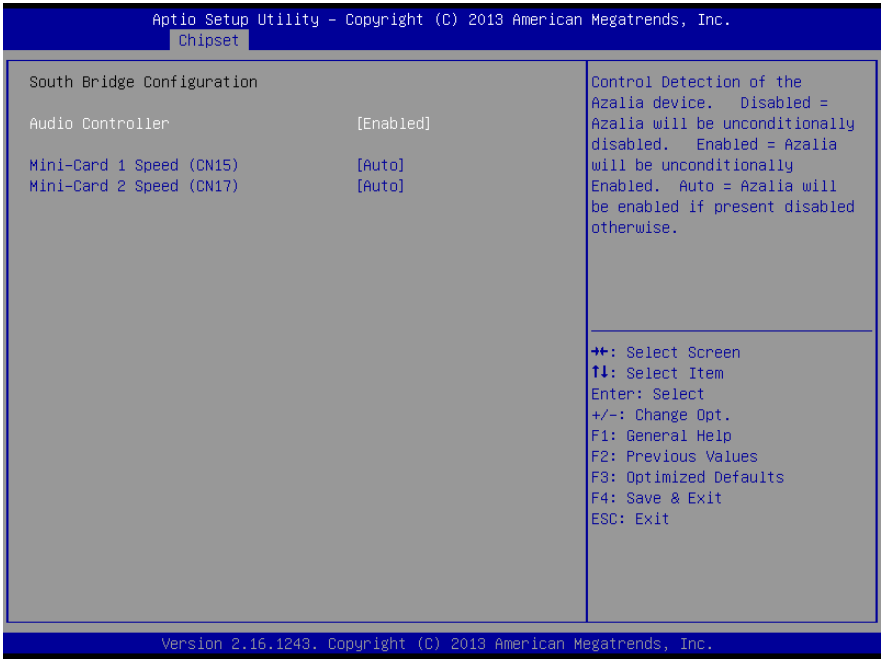
DVMT Pre-Allocated	64M	Optimal Default, Failsafe Default
	96M	
	128M	
	160M ...	
	512M	
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.		
DVMT Total Gfx Mem	128MB	Optimal Default, Failsafe Default
	256MB	
	Max	
Select DVMT 5.0 Total Graphics Memory size used by the Internal Graphics Device.		
Primary IGFX Boot Display	VBIOS Default	Optimal Default, Failsafe Default
	CRT	
	DP/HDMI	

Select the Video Device which will be activated during POST. This has no effect if external graphics present. Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display

Secondary IGFX Boot Display	Disabled	Optimal Default, Failsafe Default
	CRT	
	DP/HDMI	

Select Secondary Display Device

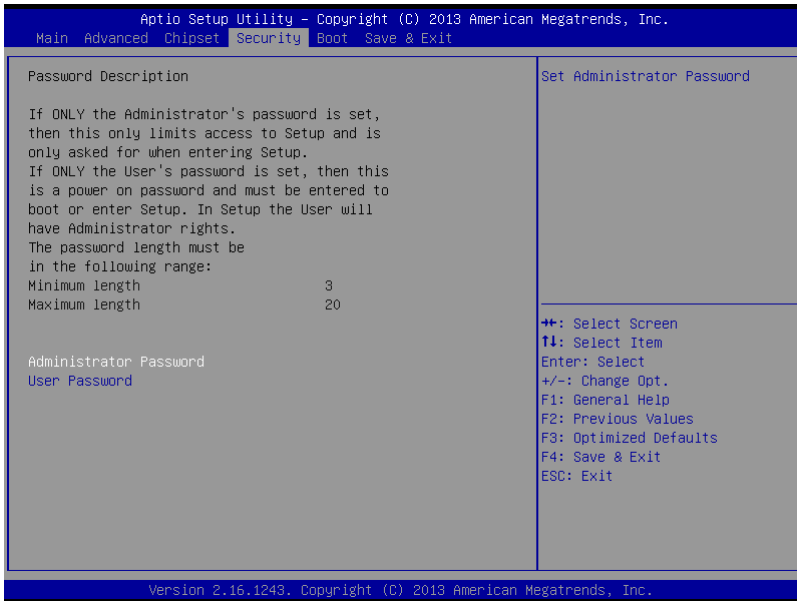
3.5.2 Chipset: South Bridge



Options summary:

Audio Controller	Enabled	Optimal Default, Failsafe Default
	Disabled	
Control Detection of the Azalia device. Disabled = Azalia will be unconditionally disabled. Enabled = Azalia will be unconditionally Enabled. Auto = Azalia will be enabled if present disabled otherwise.		
Mini-Card 1 Speed (CN15)	Auto	Optimal Default, Failsafe Default
	Gen 2	
	Gen 1	
Configure PCIe Port Speed		
Mini-Card 2 Speed (CN17)	Auto	Optimal Default, Failsafe Default
	Gen 2	
	Gen 1	
Configure PCIe Port Speed		

3.6 Setup submenu: Security



Change User/Administrator Password

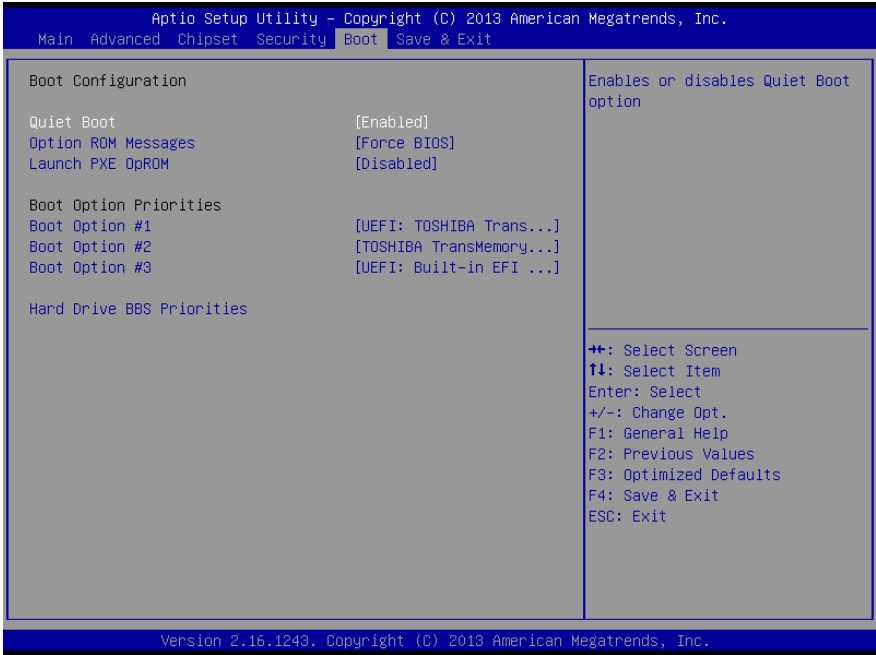
You can set a User Password once an Administrator Password. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

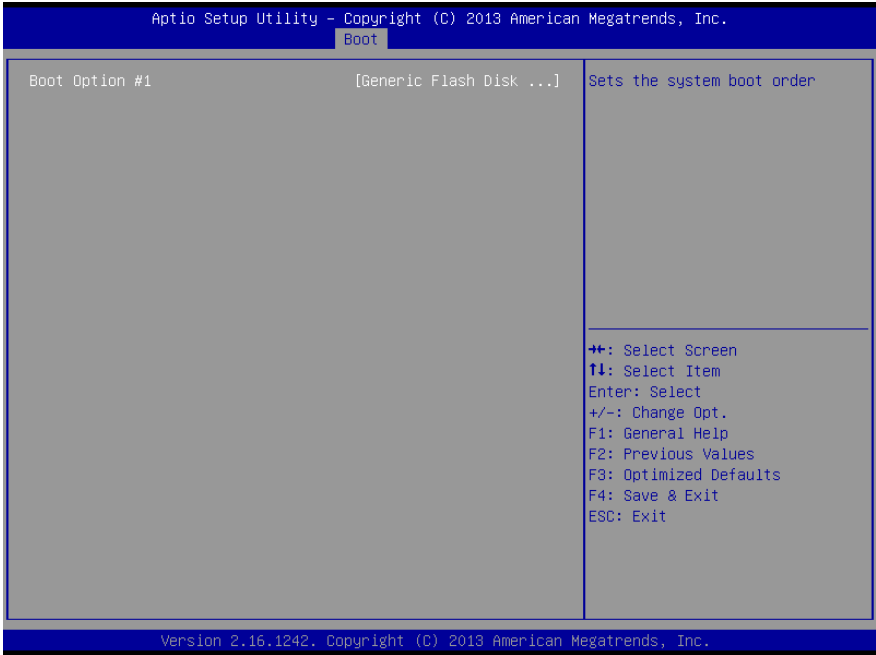
3.7 Setup submenu: Boot



Options summary:

Quiet Boot	Disabled	Default
	Enabled	
En/Disable showing boot logo.		
Option ROM Messages	Force BIOS	Default
	Keep Current	
Set display mode for Option ROM		
Launch PXE OpROM	Disabled	Default
	Enabled	
Controls the execution of LAN PXE OpROM		

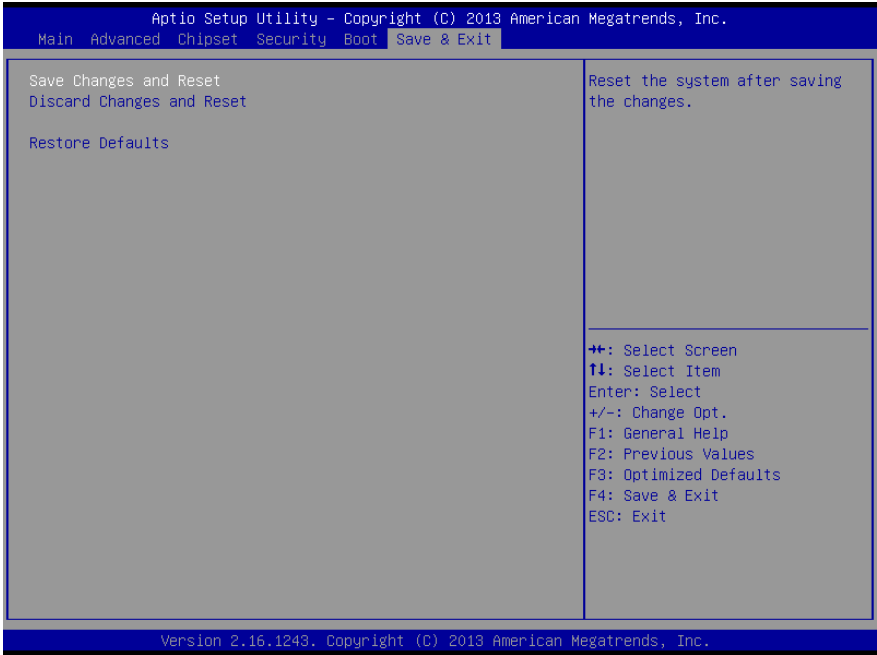
3.7.1 Boot: BBS Priorities



Options summary:

Quiet Boot	Disabled	Default
	Enabled	
En/Disable showing boot logo.		
Option ROM Messages	Force BIOS	Default
	Keep Current	
Set display mode for Option ROM		
Launch PXE OpROM	Disabled	Default
	Enabled	
Controls the execution of LAN PXE OpROM		

3.8 Setup submenu: Save & Exit



Chapter 4

Drivers Installation

4.1 Product CD/DVD

The BOXER-6313U comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

Step 1 – Install Chipset Driver

1. Open the **Step 1 - Chipset** folder followed by **SetupChipset.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 2 – Install Graphics Driver

1. Open the **Step 2 - Graphics** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 3 –Install LAN Driver

1. Open the **Step 3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

Step 4 –Install Audio Driver

1. Open the **Step 4 - AUDIO** folder followed by the **.exe** file

2. Follow the instructions
3. Drivers will be installed automatically

Step 5 –Install CAN Bus Driver

1. Open **Device Manager**
2. Right click on the device with the **exclamation mark** and select **Properties**
3. Go to the **Driver tab** and select **Update Drivers**
4. Select manual install and browse to the driver's directory
5. Confirm and drivers will be installed automatically

Step 6 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **Step 6 – USB3.0** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

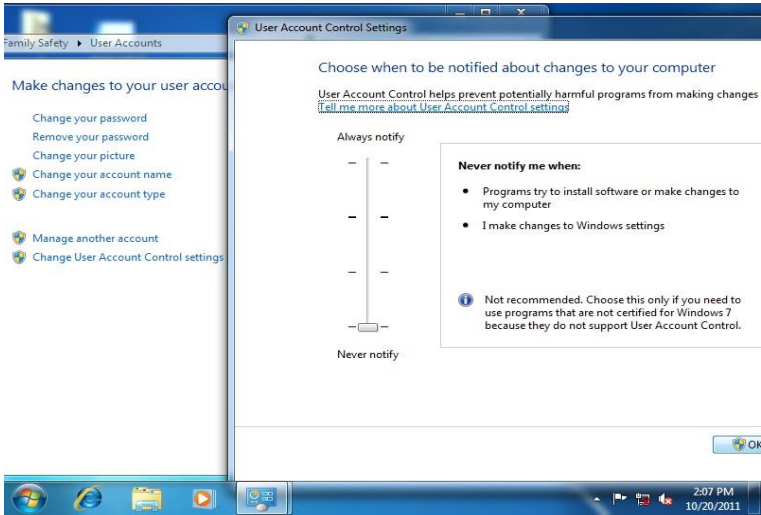
Step 7 – Install MBI Driver (Windows 8.1 only, optional)

1. Open the **Step 7 – MBI (Optional)** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

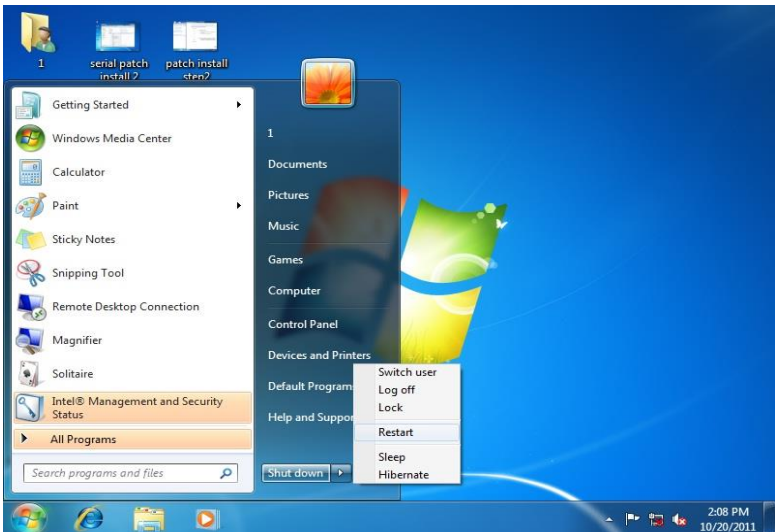
Step 8 – Install Serial Port Driver (Optional)

For Windows 7:

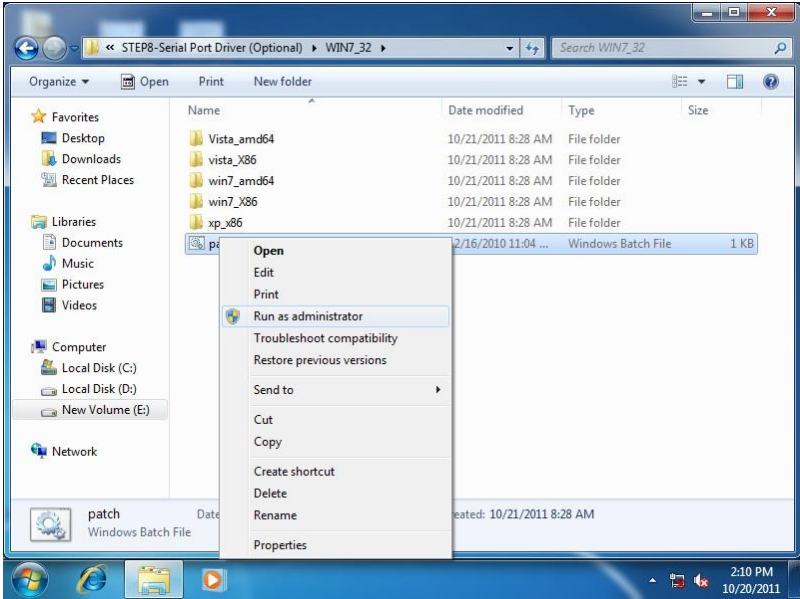
1. Change User Account Control settings to **Never notify**



2. Reboot and log in as administrator

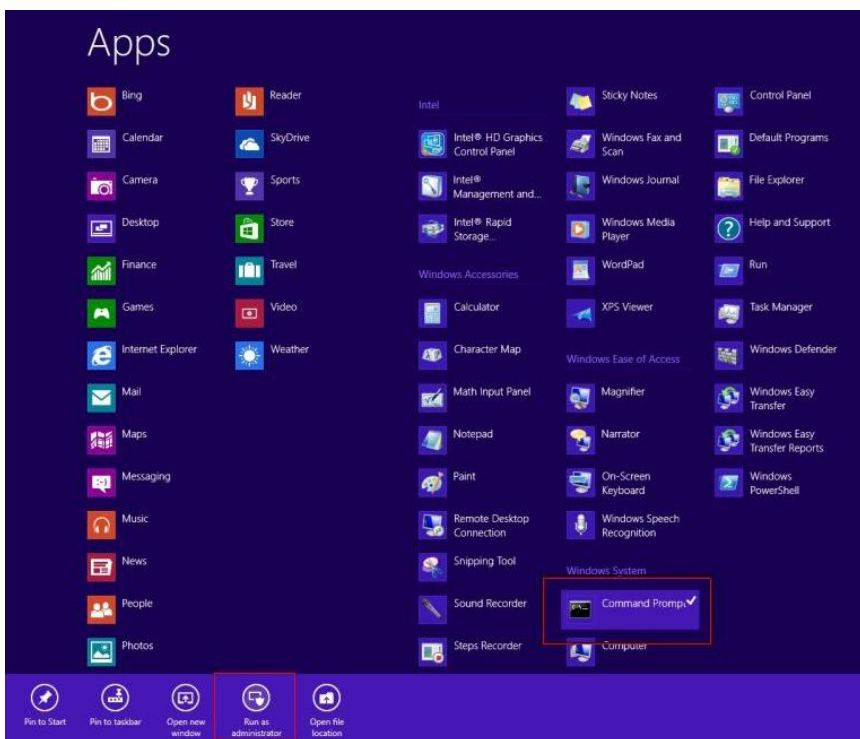


3. Run patch.bat as administrator

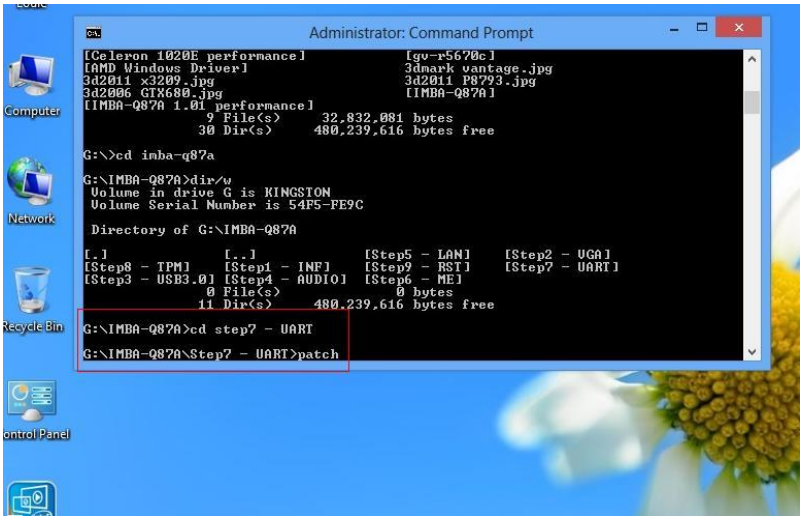


For Windows 8:

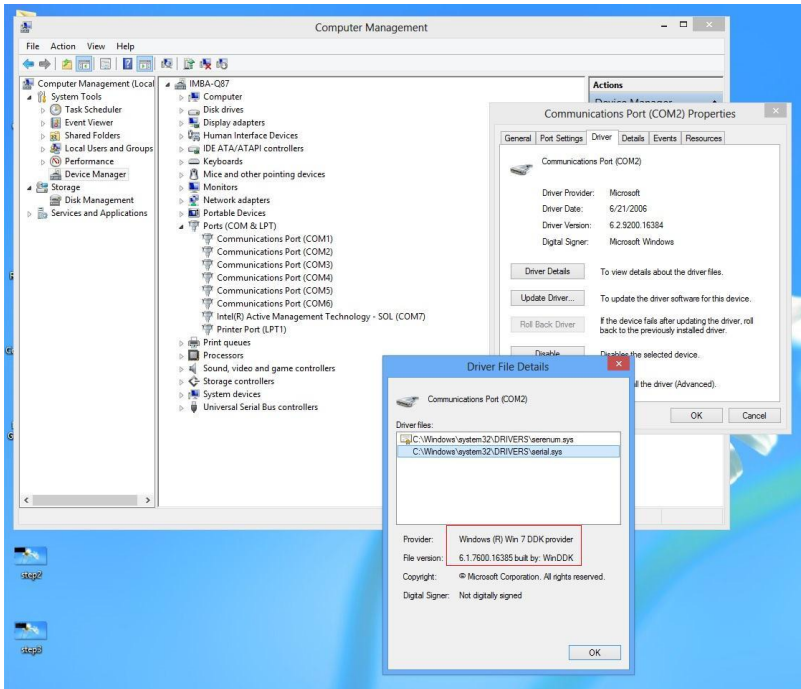
1. Open the Apps Screen, right click on the **Command Prompt** tile and select **Run as Administrator**



2. To install the driver (patch.bat), you will first have to locate the file in command prompt. To do that, go to the folder in which the file resides by entering **cd (file path)** eg: if the file is in a folder named abc in c drive, enter `cd c:\abc` (screenshot for reference only)
3. You are now at the folder where the file is located. Enter the **patch.bat** to open and install the drivers.



4. Reboot after installation completes.
5. To confirm the installation, go to Device Manager, expand the Ports (COM & LPT) tree and double click on any of the COM ports to open its properties. Go to the Driver tab, select Driver Details and click on **serial.sys**, you should see its provider as **Windows (R) Win 7 DDK Provider**.



Step 9 – Install Touch Driver (optional)

1. Open the **Step 9 –PenMount Touch 6000 (Optional)** folder followed by **Setup.exe**
2. Follow the instructions
3. Drivers will be installed automatically

Step 10 – Install GPS Driver (optional)

1. Open the **Step 10 – GPS (Optional)** folder and open both **.exe** files
2. Follow the instructions
3. Drivers will be installed automatically

Appendix A

Watchdog Timer Programming

A.1 Watchdog Timer Initial Program

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Watchdog relative register table					
	LDN	Register	BitNum	Value	Note
Timer Counter	0x07(Note3)	0xF6(Note4)		(Note24)	Time of watchdog timer (0~255) This register is byte access
Counting Unit	0x07(Note5)	0xF5(Note6)	3(Note7)	0(Note8)	Select time unit. 0: second 1: minute
Watchdog Enable	0x07(Note9)	0xF5(Note10)	5(Note11)	1(Note12)	0: Disable 1: Enable
Timeout Status	0x07(Note13)	0xF5(Note14)	6(Note15)	1	1: Clear timeout status
Output Mode	0x07(Note16)	0xF5(Note17)	4(Note18)	1(Note19)	Select WDTRST# output mode 0: level 1: pulse
WDTRST output	0x07(Note20)	0xFA(Note21)	0(Note22)	1(Note23)	Enable/Disable time out output via WDTRST# 0: Disable 1: Enable

```

*****
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex //This parameter is represented from Note1
#define byte   SIOData //This parameter is represented from Note2
#define void   IOWriteByte(byte IOPort, byte Value);
#define byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN //This parameter is represented from Note3
#define byte   TimerReg //This parameter is represented from Note4
#define byte   TimerVal // This parameter is represented from Note24
#define byte   UnitLDN //This parameter is represented from Note5
#define byte   UnitReg //This parameter is represented from Note6
#define byte   UnitBit //This parameter is represented from Note7
#define byte   UnitVal //This parameter is represented from Note8
#define byte   EnableLDN //This parameter is represented from Note9
#define byte   EnableReg //This parameter is represented from Note10
#define byte   EnableBit //This parameter is represented from Note11
#define byte   EnableVal //This parameter is represented from Note12
#define byte   StatusLDN // This parameter is represented from Note13
#define byte   StatusReg // This parameter is represented from Note14
#define byte   StatusBit // This parameter is represented from Note15
#define byte   ModeLDN // This parameter is represented from Note16
#define byte   ModeReg // This parameter is represented from Note17
#define byte   ModeBit // This parameter is represented from Note18
#define byte   ModeVal // This parameter is represented from Note19
#define byte   WDTRstLDN // This parameter is represented from Note20
#define byte   WDTRstReg // This parameter is represented from Note21
#define byte   WDTRstBit // This parameter is represented from Note22
#define byte   WDTRstVal // This parameter is represented from Note23
*****

```

```
*****
VOID Main(){
    // Procedure : AaeonWDTConfig
    // (byte)Timer : Time of WDT timer.(0x00~0xFF)
    // (boolean)Unit : Select time unit(0: second, 1: minute).
    AaeonWDTConfig();

    // Procedure : AaeonWDTEnable
    // This procedure will enable the WDT counting.
    AaeonWDTEnable();
}
*****
```



```

*****
// Procedure : AaeonWDTEnable
VOID  AaeonWDTEnable (){
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID  AaeonWDTConfig (){
    // Disable WDT counting
    WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
    // Clear Watchdog Timeout Status
    WDTClearTimeoutStatus();
    // WDT relative parameter setting
    WDTParameterSetting();
}

VOID  WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
    SIOBitSet(LDN, Register, BitNum, Value);
}

VOID  WDTParameterSetting(){
    // Watchdog Timer counter setting
    SIOByteSet(TimerLDN, TimerReg, TimerVal);
    // WDT counting unit setting
    SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
    // WDT output mode setting, level / pulse
    SIOBitSet(ModelLDN, ModeReg, ModeBit, ModeVal);
    // Watchdog timeout output via WDTRST#
    SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID  WDTClearTimeoutStatus(){
    SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*****

```

```
*****
VOID  SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

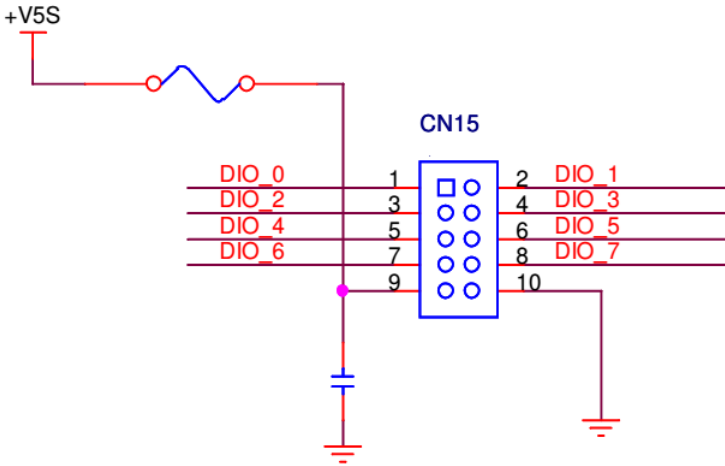
    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

Appendix B

Digital I/O Ports

B.1 Electrical Specifications for Digital I/O Ports



GPIO50	DIO_0
GPIO51	DIO_1
GPIO52	DIO_2
GPIO53	DIO_3
GPIO54	DIO_4
GPIO55	DIO_5
GPIO56	DIO_6
GPIO57	DIO_7

B.2 DIO Programming

The BOXER-6163 utilizes FINTEK F81866 chipset as its Digital I/O controller. Below are the procedures to complete its configuration. AAEON initial DI/O program is also attached for developing customized program for your application.

There are three steps to complete the configuration setup:

- (1) Enter the MB PnP Mode
- (2) Modify the data of configuration registers
- (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.

B.3 Digital I/O Register

Table 1 : SuperIO relative register table		
	Default Value	Note
Index	0x2E(Note1)	SIO MB PnP Mode Index Register 0x2E or 0x4E
Data	0x2F(Note2)	SIO MB PnP Mode Data Register 0x2F or 0x4F

Table 2 : Digital Input relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Pin Status	0x06(Note3)	0xA2(Note4)	0(Note5)		GPIO50
DIO-2 Pin Status	0x06(Note6)	0xA2(Note7)	1(Note8)		GPIO51
DIO-3 Pin Status	0x06(Note9)	0xA2(Note10)	2(Note11)		GPIO52
DIO-4 Pin Status	0x06(Note12)	0xA2(Note13)	3(Note14)		GPIO53
DIO-5 Pin Status	0x06(Note15)	0xA2(Note16)	4(Note17)		GPIO54
DIO-6 Pin Status	0x06(Note18)	0xA2(Note19)	5(Note20)		GPIO55
DIO-7 Pin Status	0x06(Note21)	0xA2(Note22)	6(Note23)		GPIO56
DIO-8 Pin Status	0x06(Note24)	0xA2(Note25)	7(Note26)		GPIO57

Table 3 : Digital Output relative register table					
	LDN	Register	BitNum	Value	Note
DIO-1 Output Data	0x06(Note27)	0xA1(Note28)	0(Note29)	(Note30)	GPIO50
DIO-2 Output Data	0x06(Note31)	0xA1(Note32)	1(Note33)	(Note34)	GPIO51
DIO-3 Output Data	0x06(Note35)	0xA1(Note36)	2(Note37)	(Note38)	GPIO52
DIO-4 Output Data	0x06(Note39)	0xA1(Note40)	3(Note41)	(Note42)	GPIO53
DIO-5 Output Data	0x06(Note43)	0xA1(Note44)	4(Note45)	(Note46)	GPIO54
DIO-6 Output Data	0x06(Note47)	0xA1(Note48)	5(Note49)	(Note50)	GPIO55
DIO-7 Output Data	0x06(Note51)	0xA1(Note52)	6(Note53)	(Note54)	GPIO56
DIO-8 Output Data	0x06(Note55)	0xA1(Note56)	7(Note57)	(Note58)	GPIO57

B.4 Digital I/O Sample Program

```
*****
// SuperIO relative definition (Please reference to Table 1)
#define byte SIOIndex //This parameter is represented from Note1
#define byte SIOData //This parameter is represented from Note2
#define void IOWriteByte(byte IOPort, byte Value);
#define byte IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte DInput1LDN // This parameter is represented from Note3
#define byte DInput1Reg // This parameter is represented from Note4
#define byte DInput1Bit // This parameter is represented from Note5
#define byte DInput2LDN // This parameter is represented from Note6
#define byte DInput2Reg // This parameter is represented from Note7
#define byte DInput2Bit // This parameter is represented from Note8
#define byte DInput3LDN // This parameter is represented from Note9
#define byte DInput3Reg // This parameter is represented from Note10
#define byte DInput3Bit // This parameter is represented from Note11
#define byte DInput4LDN // This parameter is represented from Note12
#define byte DInput4Reg // This parameter is represented from Note13
#define byte DInput4Bit // This parameter is represented from Note14
#define byte DInput5LDN // This parameter is represented from Note15
#define byte DInput5Reg // This parameter is represented from Note16
#define byte DInput5Bit // This parameter is represented from Note17
#define byte DInput6LDN // This parameter is represented from Note18
#define byte DInput6Reg // This parameter is represented from Note19
#define byte DInput6Bit // This parameter is represented from Note20
#define byte DInput7LDN // This parameter is represented from Note21
#define byte DInput7Reg // This parameter is represented from Note22
#define byte DInput7Bit // This parameter is represented from Note23
#define byte DInput8LDN // This parameter is represented from Note24
#define byte DInput8Reg // This parameter is represented from Note25
#define byte DInput8Bit // This parameter is represented from Note26
*****
```

```

*****
// Digital Output control relative definition (Please reference to Table 3)
#define byte DOutput1LDN // This parameter is represented from Note27
#define byte DOutput1Reg // This parameter is represented from Note28
#define byte DOutput1Bit // This parameter is represented from Note29
#define byte DOutput1Val // This parameter is represented from Note30
#define byte DOutput2LDN // This parameter is represented from Note31
#define byte DOutput2Reg // This parameter is represented from Note32
#define byte DOutput2Bit // This parameter is represented from Note33
#define byte DOutput2Val // This parameter is represented from Note34
#define byte DOutput3LDN // This parameter is represented from Note35
#define byte DOutput3Reg // This parameter is represented from Note36
#define byte DOutput3Bit // This parameter is represented from Note37
#define byte DOutput3Val // This parameter is represented from Note38
#define byte DOutput4LDN // This parameter is represented from Note39
#define byte DOutput4Reg // This parameter is represented from Note40
#define byte DOutput4Bit // This parameter is represented from Note41
#define byte DOutput4Val // This parameter is represented from Note42
#define byte DOutput5LDN // This parameter is represented from Note43
#define byte DOutput5Reg // This parameter is represented from Note44
#define byte DOutput5Bit // This parameter is represented from Note45
#define byte DOutput5Val // This parameter is represented from Note46
#define byte DOutput6LDN // This parameter is represented from Note47
#define byte DOutput6Reg // This parameter is represented from Note48
#define byte DOutput6Bit // This parameter is represented from Note49
#define byte DOutput6Val // This parameter is represented from Note50
#define byte DOutput7LDN // This parameter is represented from Note51
#define byte DOutput7Reg // This parameter is represented from Note52
#define byte DOutput7Bit // This parameter is represented from Note53
#define byte DOutput7Val // This parameter is represented from Note54
#define byte DOutput8LDN // This parameter is represented from Note55
#define byte DOutput8Reg // This parameter is represented from Note56
#define byte DOutput8Bit // This parameter is represented from Note57
#define byte DOutput8Val // This parameter is represented from Note58
*****

```



```
*****
VOID Main(){
    Boolean PinStatus ;

    // Procedure : AaeonReadPinStatus
    // Input :
    //     Example, Read Digital I/O Pin 3 status
    // Output :
    //     InputStatus :
    //         0: Digital I/O Pin level is low
    //         1: Digital I/O Pin level is High
    PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

    // Procedure : AaeonSetOutputLevel
    // Input :
    //     Example, Set Digital I/O Pin 6 level
    AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit,
DOutput6Val);
}
*****
```

```
*****
Boolean  AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
    Boolean PinStatus ;

    PinStatus = SIOBitRead(LDN, Register, BitNum);
    Return PinStatus ;
}
VOID  AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
    ConfigToOutputMode(LDN, Register, BitNum);
    SIOBitSet(LDN, Register, BitNum, Value);
}
*****
```

```
*****
VOID  SIOEnterMBPnPMode(){
    IOWriteByte(SIOIndex, 0x87);
    IOWriteByte(SIOIndex, 0x87);
}

VOID  SIOExitMBPnPMode(){
    IOWriteByte(SIOIndex, 0xAA);
}

VOID  SIOSelectLDN(byte LDN){
    IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
    IOWriteByte(SIOData, LDN);
}

VOID  SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(byte LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= ~(1 << BitNum);
    TmpValue |= (Value << BitNum);
    IOWriteByte(SIOData, TmpValue);
    SIOExitMBPnPMode();
}

VOID  SIOByteSet(byte LDN, byte Register, byte Value){
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    IOWriteByte(SIOData, Value);
    SIOExitMBPnPMode();
}
*****
```

```

*****
Boolean  SIOBitRead(byte LDN, byte Register, byte BitNum){
    Byte TmpValue;

    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, Register);
    TmpValue = IOReadByte(SIOData);
    TmpValue &= (1 << BitNum);
    SIOExitMBPnPMode();
    If(TmpValue == 0)
        Return 0;
    Return 1;
}
VOID  ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
    Byte TmpValue, OutputEnableReg;

    OutputEnableReg = Register-1;
    SIOEnterMBPnPMode();
    SIOSelectLDN(LDN);
    IOWriteByte(SIOIndex, OutputEnableReg);
    TmpValue = IOReadByte(SIOData);
    TmpValue |= (1 << BitNum);
    IOWriteByte(SIOData, OutputEnableReg);
    SIOExitMBPnPMode();
}
*****

```