

ARES-WHIO

Server Board

User's Manual 3rd Ed

Last Updated: August 11, 2022

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Packing List

Before setting up your product, please make sure the following items have been shipped:

ltem		Quantity
•	ARES-WHI0 server board	1
•	CPU carrier	1
•	I/O Cable	2
•	I/O Shield	1

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

- 1. All cautions and warnings on the device should be noted.
- 2. Make sure the power source matches the power rating of the device.
- Position the power cord so that people cannot step on it. Do not place anything over the power cord.
- Always completely disconnect the power before working on the system's hardware.
- No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
- 6. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
- 7. Always disconnect this device from any AC supply before cleaning.
- 8. While cleaning, use a damp cloth instead of liquid or spray detergents.
- 9. Make sure the device is installed near a power outlet and is easily accessible.
- 10. Keep this device away from humidity.
- 11. Place the device on a solid surface during installation to prevent falls
- 12. Do not cover the openings on the device to ensure optimal heat dissipation.
- 13. Watch out for high temperatures when the system is running.
- 14. Do not touch the heat sink or heat spreader when the system is running
- 15. Never pour any liquid into the openings. This could cause fire or electric shock.
- As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.

- 17. If any of the following situations arises, please the contact our service personnel:
 - i. Damaged power cord or plug
 - ii. Liquid intrusion to the device
 - iii. Exposure to moisture
 - iv. Device is not working as expected or in a manner as described in this manual
 - v. The device is dropped or damaged
 - vi. Any obvious signs of damage displayed on the device

DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.



This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

Caution:

There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.

Attention:

Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte. Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage. 产品中有毒有害物质或元素名称及含量

AAEON Main Board/ Daughter Board/ Backplane

			有	毒 有害物质耳	成元素	
部件名称	铅	汞	镉	六价铬	多溴联苯	多溴二苯醚
	(Pb)	(Hg)	(Cd)	(Cr(VI))	(PBB)	(PBDE)
印刷电路板				0	0	0
及其电子组件	U	U		0	0	0
外部信号				0		0
连接器及线材	U			0	0	0
O:表示该有毒有害物 SJ/T 11363-2006 材	:表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006标准规定的限量要求以下。					
· 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。						

备注:此产品所标示之环保使用期限,系指在一般正常使用状况下。

Poisonous or Hazardous Substances or Elements in Products

AAEON Main Board/ Daughter Board/ Backplane

	Poisonous or Hazardous Substances or Elements					
Component	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCB & Other Components	0	0	0	0	0	0
Wires & Connectors for External Connections	0	0	0	0	0	0

O: The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

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Chapter 1

Product Specifications

1.1 Specifications

System	
Form Factor	ATX Sever Board Whitely Platform
Processor	Single Intel $\ensuremath{^{\textcircled{@}}}$ Xeon $\ensuremath{^{\textcircled{@}}}$ Processor Ice Lake-SP
	processor, supports up to 270W
System Memory	DDR4 2666MHz R-DIMM Slot x 6, supports
	up to 192GB (32GB per DIMM)
Chipset	Intel®C621A
Ethernet	Intel® i210 Gigabit Ethernet x 2
СОМ	RS-232 x 1
BIOS	AMI BIOS
Serial ATA	SATA II port x 8, supports RAID 0, 1, 5,10
Audio and VGA	1
Expansion Interface	PCIE 1: PCIe x16 (Gen4 x16) slot x 1
	PCIE 2: PCIe x8 (Gen3 x4) slot x 1
	PCIE 3: PCIe x16 (Gen4 x16) slot x 1
	PCIE 4: PCIe x8 (Gen4 x4) slot x 1
	PCIE 5: PCIe x16 (Gen4 x16) slot x 1
	PCIE 6: PCIe x8 (Gen3 x4) slot x 1
	PCIE 7: PCIe x8 (Gen4 x8) slot x 1
Watchdog Timer	1~255 steps by software programming
RTC	Internal RTC
System Fan	4-Pin fan headers x 5 (up to 5 fans)
Front I/O Panel	N/A

System	
Rear I/O Panel	USB 3.0 x 6
	1Gb RJ45 LAN x 2
	AUDIO In/Out x 1
	VGA x 1
Color	N/A
Power Supply	ATX
Dimension	12.0" x 9.6" (305mm × 244 mm)
Power Consumption	269W (Based on Intel® Xeon® Platinum
	8352S)
MTBF (Hours)	292,321

Display	
Chipset	SM750
Graphic Engine	N/A
Resolution	1920x1080 (WIN Server 2019)
	800x600 (CentOS 7.3)
Connector	VGA
I/O	
Serial Port	RS-232 x 1
K/B and Mouse	N/A
USB	USB 3.0 x 6
Environmental	
Operating Temperature	0°C ~ 60°C (32°F ~ 140°F)
Storage Temperature	-4°F ~ 140°F (-20°C ~ 60°C)
Operating Humidity	10%~80% relative humidity, non-condensing
Storage Humidity	10%~80% @40°C; non-condensing

Chapter 2

Hardware Information

2.1 Dimensions

Component Side



Solder Side



2.2 Jumpers and Connectors



Note:

- For a fully configured system, we recommend that you use a power supply unit (PSU) that complies with ATX 12V Specification 2.0 (or later version) and provides a minimum power of 500W.
- We recommend that you use a PSU with a higher power output when configuring a system with more power-consuming devices. The system may become unstable or may not boot up if the power is inadequate.
- If you want to use two or more high-end PCIe x16 cards please connect ATX3, and use a PSU with 1000W power or above to ensure the system stability.

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2.3 List of Jumpers

Please refer to the table below for all of the board's jumpers that you can configure for your application

Label	Function
CMOS1	RTC Reset
JP1	Auto Power Button
JP2	ME Recover

2.3.1 RTC Reset (CMOS1)



Normal



Clear CMOS

2.3.2 Auto PWRBTN Selection (JP1)





Normal



2.4 List of Connectors

Please refer to the table below for all of the board's connectors that you can configure for your application

Label	Function
DIO1	Digital I/O
CN5	USB2.0 Port
FP1	Front Panel Pin Header
CPU_FAN1/2	CPU_FAN1
SYS_FAN3~5	CPU_FAN2
CN6	M.2 Key-M 2280
Sata1 ~ Sata8	SATA Port Connector
ATX1	24-Pin ATX Power Connector
ATX2/ATX3	8-Pin 12V Power Connector
PCIE1~PCIE7	PCIE 1: PCIe x16 (Gen4 x16) slot PCIE 2: PCIe x8 (Gen3 x4) slot PCIE 3: PCIe x16 (Gen4 x16) slot PCIE 4: PCIe x8 (Gen4 x4) slot PCIE 5: PCIe x16 (Gen4 x16) slot PCIE 6: PCIe x8 (Gen3 x4) slot PCIE 7: PCIe x8 (Gen4 x8) slot
DDR3_IPMI1 Note 2	IPMI Connector (AAEON IPMI only)
CN4	IPMI LAN only
CN14 Note 2	IPMI LAN Internal Connector.
CN2/CN3	USB3.0+LAN Connector
VGA1	VGA+COM Connector
CN15	Audio Connector
U211	LGA4189 Whitley CPU
DIMM1~8	DDR4 Slot
CN9	Case Open

Note 1: CN1/CN5/CN7/CN8/CN10/CN11/CN12/LPC1 are for Debug.

Note 2: CN14 & DDR3 are for future AAEON IPMI and only available on a project basis.

Note 3: PCIE2, PCIE4, PCIE6 are PCIe slots with x4 lanes. PCIE6 connects to PCH.

2.4.1 Digital I/O: 2.0mm Pin Header 2x5P (DIO1)



Pin	Signal	Signal Type
1	DIO0	Input / Output
2	DIO1	Input / Output
3	DIO2	Input / Output
4	DIO3	Input / Output
5	DIO4	Input / Output
6	DIO5	Input / Output
7	DIO6	Input / Output
8	DIO7	Input / Output
9	+3.3V	PWR
10	GND	GND



Pin	Signal	Signal Type
1	+5V_USB	PWR
2	GND	GND
3	USBP_1N	DIFF
4	GND	GND
5	USBP_1P	DIFF
6	USBP_2P	DIFF
7	GND	GND
8	USBP_2N	DIFF
9	GND	GND
10	+5V_USB	PWR

2.4.3 Front Panel Pin Header (FP1)



Pin	Signal	Signal Type
1	Power On Button(+)	Input
2	Reset Switch (+)	Input
3	Power On Button(-)	GND
4	Reset Switch (-)	GND
5	HDD LED (+)	Output

6	Power LED(+)	POWER
7	HDD LED (-)	Output
8	Power LED(-)	GND

2.4.4 Case Open (CN9)

Pin	Signal	Signal Type	
1	CASEOPEN#	Input	
2	GND	GND	

1___

Chapter 3

AMI BIOS Setup

3.1 System Test and Initialization

The board uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

Main - Date and time can be set here. Press <Tab> to switch between date elements

Advanced - Enable/ Disable boot option for legacy network devices

Chipset - For hosting bridge parameters

Boot - Enable/ Disable quiet Boot Option

Security - The setup administrator password can be set here

Save & Exit – Save your changes and exit the program

3.3 Setup Submenu: Main

Main Advanced Platform Configurat	Aptio Setup – AMI ion Socket Configuration	Server Mgmt Security Boot →
BIOS Information ARES-WHIO R1.1 (K770AM11)(11/17/	2021)	Set the Date. Use Tab to switch between Date elements.
BIOS Vendor Compliancy	American Megatrends UEFI 2.8; PI 1.7	Year: 1998-9999 Wonths: 1-12 Days: Dependent on month
System Date System Time	[Fri 12/10/2021] [16:13:41]	Range of Years may vary.
Access Level	Administrator	
		++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Chapter 3 – AMI BIOS Setup

3.4 Setup Submenu: Advanced

Aptio Setup – AMI Main <mark>Advanced </mark> Platform Configuration Socket Configuration	Server Mgmt Security Boot 🕨
 Main Advanced Platform Configuration Socket Configuration Trusted Computing Handware Monitor SID Configuration PCI Subsystem Settings Serial Port Console Redirection NVMe Configuration AAEON Features Power Management Digital IO Port Configuration Case Open Configuration 	<pre>the second second</pre>
Version 2 22 1282 Convright (C) 202	ESC: Exit

3.4.1 Trusted Computing

Advanced	Aptio Setup — AMI	
TFM 2.0 Device Found Firmware Version: Vendor:	5.63 IFX	Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and
Active PCR banks Available PCR banks	SHA-1,SHA256 SHA-1,SHA256	available.
SHA-1 PCR Bank SHA256 PCR Bank	[Enabled] [Enabled]	
Platform Hierarchy Storage Hierarchy	[Enabled]	++: Select Screen
Endorsement Hierarchy TPM 2.0 UEFI Spec Version Physical Presence Spec Version TPM 2.0 InterfaceType Device Select	[Enabled] [TCG_2] [1.3] [TIS] [Auto]	T∔: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values
		F3: Uptimized Defaults F4: Save & Exit ESC: Exit

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Options Summary		
Security Device	Enable	Optimal Default, Failsafe Default
Support	Disable	
Enables or Disables B	IOS support for security device	. O.S. will not show Security Device.
TCG EFI protocol and	INT1A interface will not be ava	ilable.
SHA-1 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SH	A-1 PCR Bank	
SHA256 PCR Bank	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SH	A256 PCR Bank.	
Pending operation	None	Optimal Default, Failsafe Default
	TPM Clear	
Schedule an Operation	on for the Security Device. NOT	E: Your Computer will reboot
during restart in orde	er to change State of Security D	evice.
Platform Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	

Enable or Disable Pla	atform Hierarchy	
Storage Hierarchy	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable Sto	orage Hierarchy	
Endorsement	Enabled	Optimal Default, Failsafe Default
Hierarchy	Disabled	
Enable or Disable En	dorsement Hierarchy	
TPM 2.0 UEFI Spec	TCG_2	Optimal Default, Failsafe Default
Version	TCG_1_2	
Select the TCH2 Spe	c Version Support.	
TCG_1_2: The Compa	atible mode for Win8/Win10	
TCG_2: Support new	TCG2 protocol and event forma	at for Win10 or later
Physical Presence	1.3	Optimal Default, Failsafe Default
Spec Version	1.2	
Select to Tell O.S. to s	support PPI Spec Version 1.2 or	1.3. Note some HCK tests might not
support 1.3		
Device Select	Auto	Optimal Default, Failsafe Default
	TPM 1.2	
	TPM 2.0	
TPM 1.2 will restrict s	upport to TPM 1.2 devices, TPM	12.0 will restrict support to TPM 2.0
devices, Auto will su	oport both with the default set 1	to TPM 2.0 devices if not found,
TPM 1.2 devices will	be enumerated.	

3.4.2 Hardware Monitor

Oduancad	Aptio Setup — AMI	
Havanceu		
CPU FAN Control CPU FAN 2 Control SYS FAN 3 Control CPU Temperature	[Disabled] [Disabled] [Disabled] : 452 %	For En/Disable CPU FAN Smart Control Enabled: FAN is running in accordance with user settings Disabled: FAN is always running with full speed
Sustem Temperature	• +40 %	
CPU FAN CPU FAN 2 System FAN 3 System FAN 4 System FAN 5 VCORE VMEM +12V +SV +1.05V SVSB	: +40 t : 3770 RPM : N/A : N/A : N/A : +1.812 V : +1.236 V : +11.236 V : +11.971 V : +4.979 V : +4.979 V : +1.020 V : +5.082 V	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit</pre>
+3.3V	: +3.297 V	ESC: Exit
3VSB	: +3.288 V	
VBAT	: +2.976 V	

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Options Summary		
CPU FAN / CPU	Disabled	
FAN 2 / SYS FAN 3	Enabled	Optimal Default, Failsafe Default
Control		
For En/Disable CPU	FAN / CPU FAN 2 / SYS FAN	3 Smart Control
Enabled: FAN is runr	ning in accordance with user	settings
Disabled: FAN is alw	ays running with full speed	
FAN Control Mode	Manual Mode	
	Automatic Mode	Optimal Default, Failsafe Default
Manual Mode: Depe	ends on PWM Duty	
Automatic Mode:FA	N Speed is depends on CPU	Temperature
PWM Duty	200	Optimal Default, Failsafe Default
Manual Mode: PWM	1 Duty value	
Range:[0 - 255]		
Spin PWM	100	Optimal Default, Failsafe Default
The PWM Duty of FA	AN Spin	
Range:[0 - 255]		

Off Control	30	Optimal Default, Failsafe Default	
Temperature			
Temperature Limit V	alue of Fan Off		
Note: Some fans ha	ve the minimum speed even	if the PWM value is 0	
Start Control	50	Optimal Default, Failsafe Default	
Temperature			
Temperature Limit V	Temperature Limit Value of FAN Start Control		
Full Speed	80	Optimal Default, Failsafe Default	
Temperature			
Temperature Limit V	alue of FAN Full Speed		
PWM Slope	5	Optimal Default, Failsafe Default	
Slope PWM value/Degree C for FAN Speed Control			
Range:[1-15]			

3.4.3 SIO Configuration

Aptio Setup - AMI Advanced	
AMI SID Driver Version : A5.16.00	View and Set Basic properties of the SIO Logical device.
<pre>Super 10 cmp Logical Device(s) configuration [*Active*] Serial Port</pre>	Channel and Device Mode.
WARNING: Logical Devices state on the left side of the control, reflects the current Logical Device state. Changes made during Setup Session will be shown after you restart the system.	
	→+: Select Screen
	↑↓: Select Item Enter: Select
	+/-: Change Upt. F1: General Help F2: Previous Values
	F3: Optimized Defaults F4: Save & Exit
	ESC: Exit
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Options Summary

Serial Port

View and Set Basic properties of the SIO Logical device. Like IO Base, IRQ Range, DMA Channel and Device Mode.

3.4.3.1 Serial Port Configuration

Advanced	Aptio Setup – AMI	
Serial Port Configuration		Enable or Disable this Logical
Use This Device		Device.
Logical Device Settings: Current : IO=3F8h; IRQ=4;		
Possible:	[Use Automatic Settings]	
WARNING: Disabling SIO Logical Devic side effects. PROCEED WITH CAUTION.	ces may have unwanted	++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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Options Summary		
Use This Device	Enabled	Optimal Default, Failsafe Default
	Disabled	
Enable or Disable this	s Logical Device.	
Possible	Use Automatic Settings	Optimal Default, Failsafe Default
	IO=3F8h; IRQ=4;	
	IO=2F8h; IRQ=3;	
Allows the user to ch	ange the device resource settin	gs. New settings will be reflected
on this setup page af	ter system restarts.	

3.4.4 PCI Subsystem Settings

Advanced	Aptio Setup – AMI	
PCI Bus Driver Version	A5.01.24	Enables or Disables 64bit capable Devices to be Decoded
PCI Devices Common Settings: Above 4G Decoding		in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).
		++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Versi	on 2.22.1282 Copyright (C)	2021 AMI
Options Summary		

Above 4G Decoding	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space		
(Only if System Supp	orts 64-bit PCI Decodina)	

3.4.5 Serial Port Console Configuration

Advanced	Aptio Setup — AMI	
COMO Console Redirection ▶ Console Redirection Settings Legacy Console Redirection ▶ Legacy Console Redirection Settings	[Enabled]	Console Redirection Enable or Disable.
Serial Port for Out-of-Band Manageme Windows Emergency Management Service Console Redirection EMS ▶ Console Redirection Settings	nt/ s (EMS) [Disabled]	++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2	.22.1282 Copyright (C) 2021	AMI
Options Summary		

Console	Enabled	Optimal Default, Failsafe Default	
Redirection	Disabled		
Console Redirection	Enable or Disable.		
Console Redirection	Settings		
The settings specify how the host computer and the remote computer (which the user			
is using) will exchange data.			
Both computers sho	ould have the same or compa	itible settings.	
Console	Enabled		
Redirection EMS	Disabled	Optimal Default, Failsafe Default	
Console Redirection	Enable or Disable.		

3.4.5.1 COM0 Console Redirection Settings

Advanced Emulation: ANSI: Extended ASCII char set. VT100: ASCII char		Antio Setup - AMT	
COMO Emulation: ANSI: Extended Console Redirection Settings ASCII char set. VT100: ASCII char set. VT100+: Extends	Advanced	HPCIO Setup - HMI	
Terminal Type[VT100+]VT100 to support color, function keys, etc. VT-UTF8: Data BitsData Bits[B]Uses UTF8 encoding to mapParity[None]Unicode chars onto 1 or more bytes.Stop Bits[1]Flow Control[None]VT-UTF8 Combo Key Support[Enabled]Recorder Mode[Disabled]Putty KeyPad[VT100]++: Select Screen 11: Select Item Enter: Select +/-: Change Opt.	Advanced COMO Console Redirection Settings Terminal Type Bits per second Data Bits Parity Stop Bits Flow Control VT-UTF8 Combo Key Support Recorder Mode Resolution 100x31 Putty KeyPad	[VT100+] [115200] [8] [None] [1] [None] [Enabled] [Disabled] [Disabled] [VT100]	Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set. VT100+: Extends VT100 to support color, function keys, etc. VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes. ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt.
F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit			F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2.22.1282 Copyright (C) 2021 AMI			

Options Summary		
Terminal Type	VT100	
	VT100+	Optimal Default, Failsafe Default
	VT-UTF8	
	ANSI	

Emulation :

ANSI : Extended ASCII char set.

VT100 : ASCII char set.

VT100+ : Extends VT100 to support color, function keys, etc.

VT-UTF8 : Uses UTF8 encoding to map Unicode.

Bits per second	9600	
	19200	
	38400	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port transmission speed. The speed must be matched on the other side.		

Long or noisy lines may require lower speeds.

Data bit 7 8 Optimal Default, Failsafe Defaul Parity None Optimal Default, Failsafe Defaul Even Odd Odd Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Q Z Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	Data hit	7	
Data Bits Parity None Optimal Default, Failsafe Default Parity None Optimal Default, Failsafe Default Even Odd Image: Comparison of the comparison of	Dala Dil	7	Optimal Default Faileafa Default
Data bits None Optimal Default, Failsafe Default Parity None Odd Even Odd Mark Space Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even Codd Mark Space A Parity bit is 0 if the num of 1's in the data bits is even. Odd Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Optimal Default, Failsafe Default Z 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	Doto Dito	0	Optimal Default, Failsale Default
Parity None Optimal Default, Pailsale Default Even Odd Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning); The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contrus uses two wires to send start/stop signals.	Dala bils	None	Optimal Default Failante Default
Even Odd Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contrus uses two wires to send start/stop signals.	Parity		Optimal Default, Failsale Default
Odd Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Optimal Default, Failsafe Defaul 2 Stop Bits 1 Optimal Default, Failsafe Defaul 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contruses two wires to send start/stop signals.		Even	
Mark Space A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Q Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contruses two wires to send start/stop signals.			
A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Optimal Default, Failsafe Defaul 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		Mark	
A Parity bit can be sent with the data bits to detect some transmission errors. Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Optimal Default, Failsafe Defaul 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		Space	
Even : parity bit is 0 if the num of 1's in the data bits is even. Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Q Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning); The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contruses two wires to send start/stop signals.	A Parity bit can be se	ent with the data bits to detect s	some transmission errors.
Odd : parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Q Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contruses two wires to send start/stop signals.	Even : parity bit is 0	if the num of 1's in the data bits	is even.
Mark: parity bit is always 1. Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Qptimal Default, Failsafe Default 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may. Flow control None None Optimal Default, Failsafe Default Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	Odd : parity bit is 0 i	t the num of 1's in the data bits	is odd.
Space: Parity bit is always 0 Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Qptimal Default, Failsafe Defaul 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contrustor uses two wires to send start/stop signals.	Mark: parity bit is alv	vays 1.	
Mark and Space Parity do not allow for error detection. They can be used as an additional data bit. Stop Bits 1 Qptimal Default, Failsafe Defaul 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.	Space: Parity bit is al	ways 0	
additional data bit. Stop Bits 1 Optimal Default, Failsafe Default 2 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.	Mark and Space Pari	ity do not allow for error detect	ion. They can be used as an
Stop Bits 1 Optimal Default, Failsafe Defaul 2 2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning, The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.	additional data bit.	T	1
2 Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning. The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Default Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contrust uses two wires to send start/stop signals.	Stop Bits	1	Optimal Default, Failsafe Default
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning) The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Default Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.		2	
The standard setting is 1 stop bit. Communication with slow devices may. Flow control None Optimal Default, Failsafe Defaul Hardware RTS/CTS Plow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.	Stop bits indicate the	e end of a serial data packet. (A	start bit indicates the beginning).
Flow control None Optimal Default, Failsafe Default Hardware RTS/CTS Hardware RTS/CTS Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.	The standard setting	is 1 stop bit. Communication w	ith slow devices may.
Hardware RTS/CTS Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow cont uses two wires to send start/stop signals.	Flow control	None	Optimal Default, Failsafe Default
Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.		Hardware RTS/CTS	
receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow contuses two wires to send start/stop signals.	Flow control can pre	vent data loss from buffer over	flow. When sending data, if the
buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow con- uses two wires to send start/stop signals.	receiving buffers are	full, a 'stop' signal can be sent t	to stop the data flow. Once the
uses two wires to send start/stop signals.	buffers are empty, a	'start' signal can be sent to re-s	tart the flow. Hardware flow control
	uses two wires to ser	nd start/stop signals.	
VT-UTF8 Combo Enabled Optimal Default, Failsafe Defaul	VT-UTF8 Combo	Enabled	Optimal Default, Failsafe Default
Key Support Disabled	Key Support	Disabled	
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.	Enable VT-UTF8 Cor	mbination Key Support for ANS	I/VT100 terminals.
Recorder Mode Disabled Optimal Default, Failsafe Defaul	Recorder Mode	Disabled	Optimal Default, Failsafe Default
Enabled		Enabled	
With this mode enabled only text will be sent. This is to capture Terminal data.	With this mode enak	oled only text will be sent. This is	s to capture Terminal data.
Resolution 100x31 Disabled Optimal Default. Failsafe Defaul	Resolution 100x31	Disabled	Optimal Default, Failsafe Default
Enabled		Enabled	
Enables or disables extended terminal resolution	Enables or disables (extended terminal resolution	
Putty KeyPad VT100 Ontimal Default Failsafe Default			
	Putty KeyPad		Uprimal Default Fallsate Default
VTEDMD6	Putty KeyPad		Optimal Default, Fallsafe Default
	Putty KeyPad	LINUX XTERMR6	Optimal Default, Failsate Default
	Putty KeyPad	LINUX XTERMR6	Optimal Default, Fallsafe Default
	Putty KeyPad	LINUX XTERMR6 SCO	Optimal Default, Fallsafe Default
V 1400	Putty KeyPad	LINUX XTERMR6 SCO ESCN	Optimal Default, Fallsafe Default

3.4.5.2 Legacy Console Redirection Settings

Advanced	Aptio Setup – AMI	
Legacy Console Redirection Settings	s	Select a COM port to display
Redirection COM Port Resolution Redirect After POST	[COMO] [80x24] [Always Enable]	redirection of Legacy OS and Legacy OPROM Messages
		<pre>H: Select Scheen H: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version	2.22.1282 Copyright (C) 2	2021 AMI
Options Summary		
Dedirection COM	\bigcirc	ntimal Dafault Failcofa Dafault

Redirection COM	СОМО	Optimal Default, Failsafe Default	
Port			
Select a COM port to	Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages		
Resolution	80x24	Optimal Default, Failsafe Default	
80x25			
On Legacy OS, the Number of Rows and Columns supported redirection			
Redirect After POST	Always Enable	Optimal Default, Failsafe Default	
BootLoader			
When Bootloader is s	selected, then Legacy Console F	Redirection is disabled before	
booting to legacy OS	. When Always Enable is selected	ed, then Legacy Console	
Redirection is enabled for legacy OS. Default setting for this option is set to Always			
Enable			

3.4.5.3 Console Redirection EMS Settings

Advanced	Aptio Setup – AMI	
Out-of-Band Mgmt Port Terminal Type EMS Bits per second EMS Flow Control EMS Data Bits EMS Parity EMS Stop Bits EMS	COMO [VT-UTF8] [115200] [None] 8 None 1	VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Ve	rsion 2.22.1282 Copyright	(C) 2021 AMI
Options Summary		

Terminal Type EMS	VT100	
	VT100+	
	VT-UTF8	Optimal Default, Failsafe Default
	ANSI	
VT-UTF8 is the prefe	rred terminal type for out-of-ba	and management. The next best
choice is VT100+ and	d then VT100. See above, in Cor	nsole Redirection Settings page, for
more Help with Term	inal Type/Emulation.	
Bits per second EMS	9600	
	19200	
	57600	
	115200	Optimal Default, Failsafe Default
Selects serial port tra	insmission speed. The speed mi	ust be matched on the other side.
Long or noisy lines n	nay require lower speeds.	
Flow Control EMS	None	Optimal Default, Failsafe Default
	Hardware RTS/CTS	
	Software Xon/Xoff	

Flow control can pre	event data loss from buffer over	flow.	
When sending data,	if the receiving buffers are full,	a 'stop' signal can be sent to stop	
the data flow. Once	the buffers are empty, a 'start' s	signal can be sent to re-start the	
flow. Hardware flow	control uses two wires to send	start/stop signals.	
Data Bits EMS	Pata Bits EMS 8 Optimal Default, Failsafe Default		
Data Bits			
Parity EMS	None	Optimal Default, Failsafe Default	
A parity bit can be s	ent with the data bits to detect	some transmission errors.	
Even: parity bit is 0 i	f the num of 1's in the data bits	is even.	
Odd: parity bit is 0 if	f num of 1's in the data bits is or	d.	
Mark: parity bit is always 1.			
Space: Parity bit is al	ways 0.		
Mark and Space Par	ity do not allow for error detect	ion.	
They can be used as	an additional data bit.		
Stop Bits EMS	1	Optimal Default, Failsafe Default	
Stop bits indicate the	e end of a serial data packet. (A	start bit indicates the beginning).	
The standard setting	is 1 stop bit. Communication w	vith slow devices may.	

3.4.6 NVMe Configuration

Aptio Setup - AMI Advanced	
NVMe Configuration	
No NVME Device Found	
	<pre>++: Select Screen tl: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.22.1282 Copyright (C) 2021	AMI

3.4.7 Power Management

Advanced	Aptio Setup – AMI	
Power Management		Select system power mode.
Power Mode Restore AC Power Loss	[ATX Type] [Last State]	
Wake Events RTC wake system from S5	[Disabled]	
		++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Version	2.22.1282	Copyrig	(ht (C) 2021	AMI

Options Summary		
Power Mode	АТХ Туре	Optimal Default, Failsafe Default
	АТ Туре	
Select power supply	r mode.	
Restore AC Power	Last State	Optimal Default, Failsafe Default
Loss	Always On	
	Always Off	
Select power state v	vhen power is re-applied afte	er a power failure.
RTC wake system	Disabled	Optimal Default, Failsafe Default
from S5	Fixed Time	
	Bypass	
Fixed Time : System	will wake on the hr :: min :: s	ec specified
Bypass: BIOS will no	t control RTC wake function o	during system shutdown

3.4.8 Digital IO Port Configuration

Advanced	Aptio Setup – AMI	
Digital IO Port Configuration		Set DID as Input or Output
DID1 Output Level DID2 Output Level DIO3 Output Level DIO4 Output Level DIO5 DID6 DID7 DID8	[Output] [High] [Output] [High] [Output] [High] [Input] [Input] [Input] [Input] [Input]	++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Versi	on 2.22.1282 Copyright (C)	2021 AMI

Options Summar	ry	
DIO Port1~4	Output	Optimal Default, Failsafe Default
	Input	
Set DIO as Input	or Output	
DIO Port1~4	High	Optimal Default, Failsafe Default
Output Level	Low	
Set output level v	when DIO pin is output	-
DIO Port5~8	Output	
	Input	Optimal Default, Failsafe Default
Set DIO as Input	or Output	
DIO Port5~8	High	Optimal Default, Failsafe Default
Output Level	Low	
Set output level v	when DIO pin is output	

3.4.9 Case Open Configuration

Advanced		Aptio Setup – A	AMI
navancea			
Case Open Configurat	ion		Case Open detecting function
Case Open Warning Chassis Opened		[Disabled] [No]	
			++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
	Version 2.2	2.1282 Copyrigh	nt (C) 2021 AMI
Options Summary			
Case Open	Disabled		Optimal Default, Failsafe Default
Warning	Enabled		

Case Open detecting function

Clear

3.5 Setup Submenu: Platform Configuration

Aptio Setup – AMI Main Advanced <mark>Platform Configuration</mark> Socket Configuration	Server Mgmt Security Boot 🔹 🕨
 PCH Configuration Server ME Configuration 	Displays and provides option to change the PCH Settings
Setup Warning: Setting items on this Screen to incorrect values may cause system to malfunction!	
	++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Version 2, 22, 1282 Conversion (P), 2021	AMT
version 2.22.1282 Copyright (C) 2021	AMT

3.5.1 PCH Configuration

PCH Configuration	SATA devices and settings
PCH SATA Configuration PCH sSATA Configuration	
	++: Select Screen
	Enter: Select +/-: Change Opt.
	F1: General Help F2: Previous Values
	F3: Uptimized Defaults F4: Save & Exit FSC: Exit

3.5.1.1 PCH SATA Configuration



Options Summary		
SATA Controller	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable SATA Controller		
Configure SATA as	AHCI	Optimal Default, Failsafe Default
	RAID	
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive		

3.5.1.2 PCH sSATA Configuration

[Enable] [Not Installed]	Enable or Disable SATA Controller
[Enable] [Not Installed] 	
[Not Installed]	
	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
Version 2.22.1282 Copyrig	ht (C) 2021 AMI
ibled	Optimal Default Failsafe Default
	Version 2.22.1282 Copyrig abled abled

3.5.2 Server ME Configuration

Aptio Setup – AM1 Platform Configuration		
General ME Configuration Oper. Firmware Version Backup Firmware Version ME Firmware Status #1 ME Firmware Status #2 Current State Error Code Recovery Cause PTT Support Suppress PTT Commands	0F:4.4.4.58 N/A 0F:4.4.4.58 0x000F0255 0x89112006 Dperational No Error N/A [Disable] [Disable]	Enable/Disable sending HMRFPO_ENABLE message to ME
HMRFPO_ENABLE Message		++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Options Summary		
HMRFPO_ENABLE	Disable	Optimal Default, Failsafe Default
Message	Enable	
Enable/Disable sending HMRFPO_ENABLE Message to ME		

3.6 Setup Submenu: Socket Configuration

Aptio Setup – Main Advanced Platform Configuration Socket Conf	AMI iguration Server Mgmt Security Boot →
 Processor Configuration Memory Configuration IIO Configuration Advanced Power Management Configuration 	Displays and provides option to change the Processor Settings
	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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3.6.1 Processor Configuration

	Aptio Setup – AMI Socket Configurati	on
Processor Configuration Processor BSP Revision	606A6 - ICX D0	Enables Hyper Threading (Software Method to Enable/Disable Logical
Processor Socket Processor ID Processor Frequency Processor Max Ratio Processor Min Ratio Microcode Revision L1 Cache RAM(Per Core) L2 Cache RAM(Per Core) L3 Cache RAM(Per Package)	SOCKET 0 SOCKET 1 000606A6* N/A 2.200GHz N/A 16H N/A 00H N/A 0D0002C0 N/A 80KB N/A 1280KB N/A 49152KB N/A	Processor Threads.
Processor O Version Hyper-Threading [ALL]	Intel(K) Xeon(K) Gold 338N CPU @ 2.20GHz [Enable]	6 ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

Options Summary		
Hyper-Threading	Disable	
[ALL]	Enable	Optimal Default, Failsafe Default
Enables Hyper Threading (Software Method to Enable/Disable Logical Processor		
threads.		

3.6.2 Memory Configuration

	Aptio Setup – AMI Socket Configuration	
Integrated Memory Controller (IMC)		Displays memory topology with Dimm population information
▶ Memory Topology		
		<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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3.6.2.1 Memory Topology



3.6.3 IIO Configuration

Aptio Setup – AMI Socket Configuration	
IIO Configuration 	Press ≪Enter≻ to bring up the Intel® Virtualization for Directed I/O (VT–d) Configuration menu.
	++: Select Screen 14: Select Item Enter: Select +/: Change Ont
	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit FSC: Fvit
	cor chit
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3.6.4 Intel® VT for Directed I/O (VT-d)

	Aptio Setup – AMI Socket Configuration	
Intel® VT for Directed I/O (VT-d)		Enable/Disable Intel® Virtualization Technology for Directed I/O (VI-d) bu
Intel® VT for Directed I/O X2APIC Opt Out	[Enable] [Disable]	<pre>birected 1/U (VI-0) by reporting the I/O device assignment to VMM through DMAR ACPI Tables. ++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

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Options Summary		
Intel® VT for	Enable	Optimal Default, Failsafe Default
Directed I/O	Disable	
Enables Hyper Threathreads.	ading (Software Method to Ei	nable/Disable Logical Processor
X2APIC Opt Out	Enable	
	Disable	Optimal Default, Failsafe Default
Enable/Disable X2APIC_OPT_OUT bit		

3.6.5 Advanced Power Management Configuration

Aptio Setup Socket Co	- AMI nfiguration
Advanced Power Management Configuration	CPU C State setting
▶ CPU C State Control	
	++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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3.6.5.1 CPU C State Control

	Aptio Setup – Socket Conf	AMI iguration
CPU C State Control		Allows Monitor and MWAIT
Enable Monitor MWAI		instructions.
		++: Select Screen ↑↓: Select Item
		Enter: Select +/-: Change Opt.
		F1: General Help F2: Previous Values
		F3: Optimized Defaults F4: Save & Exit
		ESC: Exit
	Version 2.22.1282 Copyrig	ht (C) 2021 AMI
Options Summary		
Enable Monitor	Disable	

Enable Monitor	Disable	
MWAIT	Enable	Optimal Default, Failsafe Default
Allows Monitor and MWAIT instructions.		

3.7 Setup Submenu: Security

	Main Advanced Platform Configurat	Aptio Setup – AMI ion Socket Configuration	Server Mgmt Security Boot 🕨
Γ	Password Description		Set Administrator Password
	If ONLY the Administrator's password then this only limits access to Setu only asked for when entering Setup. If ONLY the User's password is set, is a power on password and must be e boot or enter Setup. In Setup the Us have Administrator rights. The password length must be in the following range:	is set, p and is then this ntered to er will	
	Maximum length	3 20	
	Administrator Password User Password		<pre>++: Select Screen 1↓: Select Item Enter: Select +/-: Change Opt.</pre>
•	Secure Boot		F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
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Change User/Administrator Password

If an Administrator Password is set, it will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

3.7.1 Secure Boot



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Options Summary			
Secure Boot	Disabled	Optimal Default, Failsafe Default	
	Enabled		
Secure Boot feature	is Active if Secure Boot is Ena	abled, Platform Key(PLK) is enrolled	
and the System is in	User mode. The mode chan	ge requires platform reset	
Secure Boot Mode	Standard		
	Custom	Optimal Default, Failsafe Default	
Secure Boot mode options: Standard or Custom.			
In Custom mode, Secure Boot Policy variables can be configured by a physically			
present user without full authentication			
Restore Factory	Force System to User Mode. Install factory default Secure Boot key		
Keys	databases.		
Reset To Setup	Delete all Secure Boot key databases from NVRAM		
Mode			

3.7.1.1 Key Management



	Aptio Setup – AMI	Security
Vendor Keys	Valid	Install factory default Secure
Factory Key Provision • Restore Factory Keys • Reset To Setup Mode • Export Secure Boot var • Enroll Efi Image	[Disabled] iables	reset and while the System is in Setup mode
Device Guard Ready ▶ Remove 'UEFI CA' from ▶ Restore DB defaults	DB	
Secure Boot variable > Platform Key(PK) > Key Exchange Keys > Authorized Signatures > Forbidden Signatures > Authorized TimeStamps > OsRecovery Signatures	Size Keys Key Source 0 0 No Keys 0 0 No Keys	<pre>++: Select Screen 11: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>

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Options Summary			
Factory Key	Disabled	Optimal Default, Failsafe Default	
Provision	Enabled		
Install factory defaul	t Secure Boot keys after the p	olatform reset and while the System is	
in Setup mode			
Restore Factory	Force System to User Mode. Install factory default Secure Boot key		
Keys	databases.		
Reset To Setup	Delete all Secure Boot key databases from NVRAM		
Mode			
Export Secure Boot	Copy NVRAM content of Secure Boot variables to files in a root		
variables	folder on a file system device		
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash		
	certificate of a PE image into Authorized Signature Database (db)		
Remove 'UEFI CA'	Device Guard ready system must not list 'Microsoft UEFI CA'		
from DB	Certificate in Authorized Signature database (db)		
Restore DB defaults	Restore DB variable to factory defaults		

Secure Boot Variables

Enroll Factory Defaults or load certificates from a file:

- 1. Public Key Certificate in:
 - a) EFI_SIGNATURE_LIST
 - b) EFI_CERT_X509 (DER encoded)
 - c) EFI_CERT_RSA2048 (bin)
 - d) EFI_CERT_SHAXXX
- 2. Authenticated UEFI Variable
- 3. EFI PE/COFF Image(SHA256)

Key Source:

Default, External, Mixed

Setup Submenu: Boot 3.8

Main Advanced	Aptio Setup – AMI Platform Configuration Socket Configuration	Server Mgmt Security Boot
Boot Configurati Quiet Boot	on (Enabled)	Enables or disables Quiet Boot option
Network Stack CSM Support	[Disabled] [Disabled]	
FIXED BOOT ORDER Boot Option #1 Boot Option #2 Boot Option #3 Boot Option #4	Priorities [UEFI Hard Disk] [UEFI NVME] [UEFI CD/DVD] [UEFI SD] [UEFI SD]	
Boot Option #5 Boot Option #6 Boot Option #7 Boot Option #8 Boot Option #9	(UEFI USB HAND UISK) (UEFI USB CD/DVD) (UEFI USB Key) (UEFI USB Floppy) (UEFI USB Lan)	++: Select Screen 11: Select Item Enter: Select +/-: Change Opt.
Boot Option #10	[UEFI Network]	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Vancias 0.00.4000 Desusidat (D) 0004.007		

Options Summary		
Quiet Boot	Disabled	
	Enabled	Optimal Default, Failsafe Default
Enable or Disable Quiet Boo	ot option.	
Network Stack	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable UEFI Netwo	rk Stack.	
CSM Support	Disabled	Optimal Default, Failsafe Default
	Enabled	
Enable/Disable CSM Suppo	rt.	
FIXED BOOT ORDER Priorities		Sets the system boot order

3.9 Setup Submenu: Save & Exit

Aptio Setup - AMI ≺ Save & Exit	
Save Options Save Changes and Reset Discard Changes and Exit Default Options Restore Defaults	Reset the system after saving the changes.
	<pre>++: Select Screen 14: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit</pre>
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Options Summary	
Save Changes and Reset	Reset the system after saving the changes.
Discard Changes and Exit	Exit system setup without saving any changes.
Restore Defaults	Restore/Load Default values for all the setup options.

Chapter 4

Driver Installation

4.1 Driver Download/Installation

Drivers for the ARES-WHI0 can be downloaded from the product page on the AAEON website by following this link:

https://www.aaeon.com/en/p/intel-ice-lake-xeon-server-board-ares-whi0

Download the driver(s) you need, extract them to their respective folders and follow the steps below to install them.

Step 1 – Install Chipset Drivers

- 1. Open the Chipset-10.1.18736.8270-Public-Server-MUP folder
- 2. Run the SetupChipset.exe in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 2 – Install Graphics Drivers

- 1. Open the SM750 WDDM2.0 v10.00.18.00-1119-sign(MS)-60028 folder
- 2. Run the setup.exe file in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 3 – Install Network Driver

- 1. Open the Intel LAN 26.6 folder, then open the Wired_driver_26.6_x64 subfolder
- 2. Run the Wired_driver_26.6_x64.exe file in the subfolder
- 3. Follow the instructions
- 4. Drivers will be installed automatically

Step 4 – Install Audio Driver

- 1. Open the Audio Driver V8978 folder
- 2. Run the Setup.exe file in the folder
- 3. Follow the instructions
- 4. Drivers will be installed automatically