# AEC-6977

Fanless Embedded Box PC

User's Manual 3rd Ed

*Last Updated: January 13, 2017*

## Copyright Notice

## Acknowledgement

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- ITE is a trademark of Integrated Technology Express, Inc.
- IBM and VGA are trademarks of International Business Machines Corporation.

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## Packing List

Before setting up your product, please make sure the following items have been shipped:

| Item | Quantity |
|---|---|
| ● AEC-6977 | 1 |
| ● Phoenix power connector | 1 |
| ● M3 x 4mm screws | 4 |
| ● 6# -32 x 10mm screws | 6 |
| ● Wallmount bracket | 2 |
| ● Product DVD with User's Manual (in pdf) and drivers | 1 |

If any of these items are missing or damaged, please contact your distributor or sales representative immediately.

## About this Document

This User's Manual contains all the essential information, such as detailed descriptions and explanations on the product's hardware and software features (if any), its specifications, dimensions, jumper/connector settings/definitions, and driver installation instructions (if any), to facilitate users in setting up their product.

Users may refer to the AAEON.com for the latest version of this document.

## Safety Precautions

Please read the following safety instructions carefully. It is advised that you keep this manual for future references

1. All cautions and warnings on the device should be noted.
2. All cables and adapters supplied by AAEON are certified and in accordance with the material safety laws and regulations of the country of sale. Do not use any cables or adapters not supplied by AAEON to prevent system malfunction or fires.
3. Make sure the power source matches the power rating of the device.
4. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
5. Always completely disconnect the power before working on the system's hardware.
6. No connections should be made when the system is powered as a sudden rush of power may damage sensitive electronic components.
7. If the device is not to be used for a long time, disconnect it from the power supply to avoid damage by transient over-voltage.
8. Always disconnect this device from any AC supply before cleaning.
9. While cleaning, use a damp cloth instead of liquid or spray detergents.
10. Make sure the device is installed near a power outlet and is easily accessible.
11. Keep this device away from humidity.
12. Place the device on a solid surface during installation to prevent falls
13. Do not cover the openings on the device to ensure optimal heat dissipation.
14. Watch out for high temperatures when the system is running.
15. Do not touch the heat sink or heat spreader when the system is running
16. Never pour any liquid into the openings. This could cause fire or electric shock.

17. As most electronic components are sensitive to static electrical charge, be sure to ground yourself to prevent static charge when installing the internal components. Use a grounding wrist strap and contain all electronic components in any static-shielded containers.
18. If any of the following situations arises, please the contact our service personnel:
    i. Damaged power cord or plug
    ii. Liquid intrusion to the device
    iii. Exposure to moisture
    iv. Device is not working as expected or in a manner as described in this manual
    v. The device is dropped or damaged
    vi. Any obvious signs of damage displayed on the device
19. DO NOT LEAVE THIS DEVICE IN AN UNCONTROLLED ENVIRONMENT WITH TEMPERATURES BEYOND THE DEVICE'S PERMITTED STORAGE TEMPERATURES (SEE CHAPTER 1) TO PREVENT DAMAGE.

## FCC Statement


This device complies with Part 15 FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

*Caution:*

*There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions and your local government's recycling or disposal directives.*

*Attention:*

*Il y a un risque d'explosion si la batterie est remplacée de façon incorrecte.*
*Ne la remplacer qu'avec le même modèle ou équivalent recommandé par le constructeur. Recycler les batteries usées en accord avec les instructions du fabricant et les directives gouvernementales de recyclage.*

## China RoHS Requirements (CN)

产品中有毒有害物质或元素名称及含量

AAEON Embedded Box PC/ Industrial System

| 部件名称 | 有毒有害物质或元素 | | | | | |
|---|---|---|---|---|---|---|
| | 铅 (Pb) | 汞 (Hg) | 镉 (Cd) | 六价铬 (Cr(VI)) | 多溴联苯 (PBB) | 多溴二苯醚 (PBDE) |
| 印刷电路板及其电子组件 | ○ | ○ | ○ | ○ | ○ | ○ |
| 外部信号连接器及线材 | ○ | ○ | ○ | ○ | ○ | ○ |
| 外壳 | ○ | ○ | ○ | ○ | ○ | ○ |
| 中央处理器与内存 | ○ | ○ | ○ | ○ | ○ | ○ |
| 硬盘 | ○ | ○ | ○ | ○ | ○ | ○ |
| 电源 | ○ | ○ | ○ | ○ | ○ | ○ |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。

X：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。

备注：
一、此产品所标示之环保使用期限，系指在一般正常使用状况下。
二、上述部件物质中央处理器、内存、硬盘、电源为选购品。

## China RoHS Requirement (EN)

Poisonous or Hazardous Substances or Elements in Products

AAEON Embedded Box PC/ Industrial System

| Component | Poisonous or Hazardous Substances or Elements | | | | | |
|---|---|---|---|---|---|---|
| | Lead (Pb) | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (Cr(VI)) | Polybrominated Biphenyls (PBB) | Polybrominated Diphenyl Ethers (PBDE) |
| PCB & Other Components | O | O | O | O | O | O |
| Wires & Connectors for External Connections | O | O | O | O | O | O |
| Chassis | O | O | O | O | O | O |
| CPU & RAM | O | O | O | O | O | O |
| Hard Disk | O | O | O | O | O | O |
| PSU | O | O | O | O | O | O |

O：The quantity of poisonous or hazardous substances or elements found in each of the component's parts is below the SJ/T 11363-2006-stipulated requirement.

X: The quantity of poisonous or hazardous substances or elements found in at least one of the component's parts is beyond the SJ/T 11363-2006-stipulated requirement.

Note: The Environment Friendly Use Period as labeled on this product is applicable under normal usage only

## Table of Contents

# Chapter 1

Product Specifications

## 1.1 Specifications

### System

| | |
|---|---|
| ● Pr°Cessor | Intel® 3rd Generation Core™ i/ Celeron® Pr°Cessor (FCBGA1023) |
| ● System Memory | 204-pin DDR3 1066/1333 MHz SODIMM x 2, up to 16 GB |
| ● Chipset | Intel® QM77 |
| ● Storage | CFast™ x 1<br>SSD/HDD: SATA 6.0 Gb/s x 2 (SATA 0, 2), SATA 3.0 Gb/s x 2 (SATA 2, 3), support RAID 0, 1, 5, 10 |
| ● Rear I/O Panel | USB 3.0 x 2<br>USB 2.0 x 2<br>RJ-45 x 2<br>RS-232 x 2<br>Mic-in, Line-in, Line-out<br>Power input x 1 |
| ● Front I/O Panel | USB3.0 x 2<br>RS-232 x 1, RS-232/422/485 x 1, optional 2.5KV Isolation ,<br>RS-232 x 6 (optional)<br>8-bit programmable DIO, optional 2.5KV Isolation 2.5KV, DO x 4 and DI x 4<br>PS/2 x 1<br>Power button x 1<br>Reset button x 1 |

| | |
|---|---|
| ● Front Indicators | LED for power status x 1 |
| | LED for HDD status x 1 |
| ● Expansion Slot | PCIe[x1] x 2 (optional) |
| | PCI x2 (optional, limited to 2.1A@12V) |
| | Mini card x2 (optional) |
| | SIM x 1 (optional) |
| ● OS Support | Windows® 10 |
| | Windows® XP Embedded |
| | Windows® XP |
| | Windows® 7 |
| | Linux Fedora 10 |

## Mechanical

| | |
|---|---|
| ● Construction | - |
| ● Mounting | Wallmount |
| ● Dimension (W x H x D) | 208 x 124.4 x 238mm (8.19" x 4.9" x 9.37") |
| ● Gross Weight | - |

## Environmental

| | |
|---|---|
| ● Operating Temperature | Without Airflow, with wide temperature Storage and RAM: |
| | -20 ~ 50°C (-4 ~ 122°F) (35W TDP CPU) |
| | -20 ~ 65°C (-4 ~ 149°F) (17W TDP CPU, not include riser card) |
| | Ambient with Airflow, with wide temperature Storage and RAM: |

| | |
|---|---|
| | -4°F ~ 140°F (-20°C ~ 60°C) (35W TDP CPU)<br>-4°F ~ 167°F (-20°C ~ 65°C) (17W TDP CPU, not include riser card |
| ● Storage Temperature | -20 ~ 70°C (-4 ~ 158°F) |
| ● Operating Humidity | - |
| ● Anti-Vibration | 3 g rms/ 5~500 Hz/ operation-CFast™;<br>1 g rms/ 5~500 Hz/ operation-HDD |
| ● Anti-Shock | 50 G peak acceleration (11 msec. duration) –CFast™ |
| ● EMC | CE/FCC Class A |

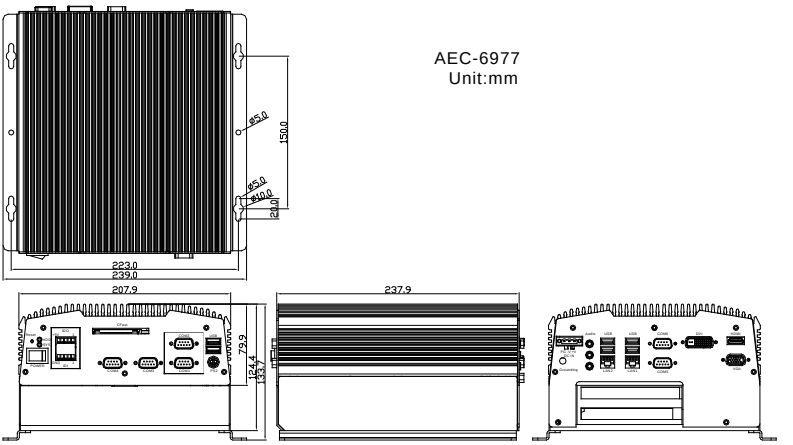
## Power Supply

| | |
|---|---|
| ● DC Input | DC-in 9~30V input, optional 100~240V |

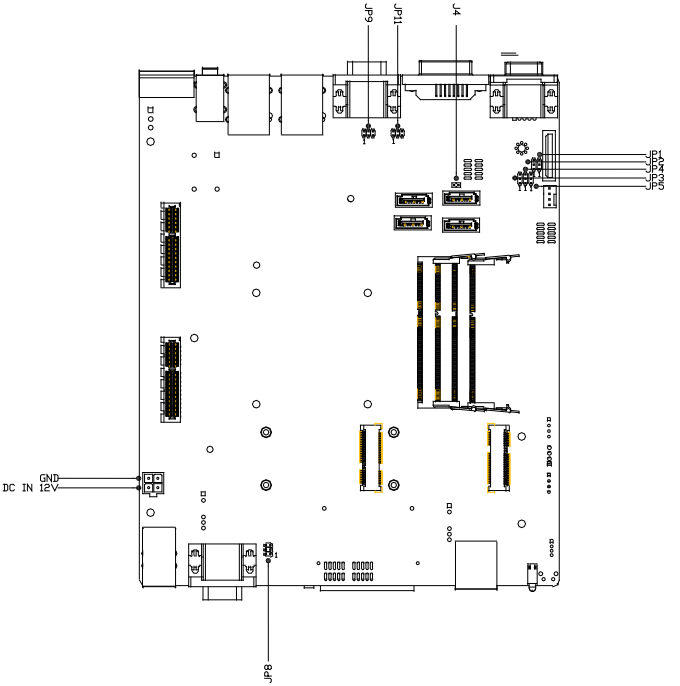
# Chapter 2

Hardware Information

## 2.1 Dimensions



## 2.2 Jumpers and connectors



## 2.3 List of Jumpers

Please refer to the table below for all of the system's jumpers that you can configure for your application

| Label | Function |
|---|---|
| JP1 | Clear CMOS |
| JP2 | Clear ME |
| JP3 | Inverter Power Selection |
| JP4 | LVDS Port Backlight Lightness Control Mode Selection |
| JP5 | LVDS Voltage Selection |
| JP8 | RS-232/422/485 Selection |
| JP9 | COM6 +12V/+5V/RING Selection |
| JP11 | COM5 +12V/+5V/RING Selection |
| J6 | Auto Power Button |

### 2.3.1 Clear CMOS Jumper (JP1)

| JP1 | Function |
|---|---|
| 1-2 | Normal (Default) |
| 2-3 | Clear CMOS |

### 2.3.2 Clear ME (JP2)

| JP2 | Function |
|---|---|
| 1-2 | Normal (Default) |
| 2-3 | Clear ME |

### 2.3.3 Inverter Power Selection (JP3)

| JP3 | Function |
|---|---|
| 1-2 | +12V (Default) |
| 2-3 | +5V |

### 2.3.4 LVDS Port Backlight Lightness Control Mode Selection (JP4)

| JP4 | Function |
|---|---|
| 1-2 | PWM MODE |
| 2-3 | VR MODE (Default) |

### 2.3.5 LCD Voltage Selection (JP5)

| JP5 | Function |
|---|---|
| 1-2 | +5V |
| 2-3 | +3.3V (Default) |

### 2.3.6 Isolation COM2 RS232/RS485/RS422 selection (JP8)

| JP8 | Function |
|---|---|
| RS232 | 1-2,3-4,5-6 close |
| RS422 | 3-4 close , 1-2 5-6 open |
| RS485 | 5-6 close , 1-2 3-4 open |

### 2.3.7 COM6 +12V/+5V/Ring Selection (JP9)

| JP9 | Function |
|---|---|
| 1-2 | +12V |
| 3-4 | +5V |
| 5-6 | Ring (Default) |

### 2.3.8 COM5 +12V/+5V/Ring Selection (JP11)

| JP11 | Function |
|---|---|
| 1-2 | +12V |
| 3-4 | +5V |
| 5-6 | Ring (Default) |

### 2.3.9 Auto Power Button (J6)

| JP6 | Function |
|---|---|
| OPEN | ATX (Default) |
| 1-2 | AT |

## 2.4 List of Connectors

Please refer to the table below for all of the system's connectors that you can configure for your application

| Label | Function |
|---|---|
| CN1 | Front Panel Connector |
| CN2 | 4-pin ATX Power +12V Connector |
| CN6 ~ CN7 | LAN / USB Connector |
| CN8 | CFast™ Connector |
| CN10 | COM3 RS-232 Box Header |
| CN11 | COM4 RS-232 Box Header |
| CN13 | COM5 / COM6 Connector |
| CN15 | VGA / HDMI Connector |
| CN16 | DVI-I Connector |
| CN17 | LVDS Connector |
| CN18 | LVDS Inverter / Backlight Connector |
| CN21 | Mini Card Connector With SIM |
| CN24 | Mini Card Connector |
| CN26/CN33 | PCIE*4 Connector |
| CN27 | USB X2 / PS2 Connector |
| CN29 | Digital I/O |
| CN30 | ISOLATION COM1 / COM2 Connector |
| CN31 | DC IN |
| PWR1 ~ PWR2 | SATA POWER |
| SATA1~SATA2 | SATA 3.0 Connector |
| SATA3~SATA4 | SATA Connector |
| DIMM1,DIMM2 | DDR3 DIMM Slot |
| USB1 | USB Box Header |

| Label | Function |
| --- | --- |
| FAN1~ FAN2 | 4 Pin Fan Connector |
| AUDIO1 | AUDIO Connector |

### 2.4.1 SATA Power (PWR1~PWR2)

| PIN | Signal |
|---|---|
| 1 | +12V |
| 2 | GND |
| 3 | GND |
| 4 | +5V |

### 2.4.2 Front Panel Connector (CN4)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Power On Button (-) | 2 | Power On Button (+) |
| 3 | HDD LED (-) | 4 | HDD LED (+) |
| 5 | SPEAKER(-) | 6 | SPEAKER(+) |
| 7 | Power LED (-) | 8 | Power LED (+) |
| 9 | Reset Switch (-) | 10 | Reset Switch (+) |

### 2.4.3 LVDS Connector (CN17)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | BKL_EN | 2 | BKL_CTL |
| 3 | LVDSVCC | 4 | GND |
| 5 | LVDSA_CLK# | 6 | LVDSA_CLK |
| 7 | LVDSVCC | 8 | GND |
| 9 | LVDSA_DATA0# | 10 | LVDSA_DATA0 |
| 11 | LVDSA_DATA1# | 12 | LVDSA_DATA1 |
| 13 | LVDSA_DATA2# | 14 | LVDSA_DATA2 |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 15 | LVDSA_DATA3# | 16 | LVDSA_DATA3 |
| 17 | LVDS_DDC_DATA | 18 | LVDS_DDC_CLK |
| 19 | LVDSB_DATA0# | 20 | LVDSB_DATA0 |
| 21 | LVDSB_DATA1# | 22 | LVDSB_DATA1 |
| 23 | LVDSB_DATA2# | 24 | LVDSB_DATA2 |
| 25 | LVDSB_DATA3# | 26 | LVDSB_DATA3 |
| 27 | LVDSVCC | 28 | GND |
| 29 | LVDSB_CLK# | 30 | LVDSB_CLK |

### 2.4.4 LVDS Inverter/ Backlight Connector (CN18)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VDD | 2 | BKL_CTL |
| 3 | GND | 4 | GND |
| 5 | BKL_EN | | |

### 2.4.5 RS-232/422/485 Pin DEFINE (COM2)

RS-232

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD | 2 | RXD |
| 3 | TXD | 4 | DTR |
| 5 | GND | 6 | DSR |
| 7 | RTS | 8 | CTS |
| 9 | RI | | |

RS-422

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TXD- | 2 | RXD+ |
| 3 | TXD+ | 4 | RXD- |
| 5 | Ground | 6 | N/C |
| 7 | N/C | 8 | N/C |
| 9 | N/C | | |

RS-485

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | D- | 2 | N/C |
| 3 | D+ | 4 | N/C |
| 5 | Ground | 6 | N/C |
| 7 | N/C | 8 | N/C |
| 9 | N/C | | |

### 2.4.6 RS-232 Box Header (COM3)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD | 2 | RXD |
| 3 | TXD | 4 | DTR |
| 5 | GND | 6 | DSR |
| 7 | RTS | 8 | CTS |
| 9 | RI | | |

### 2.4.7 RS-232 Box Header (COM4)

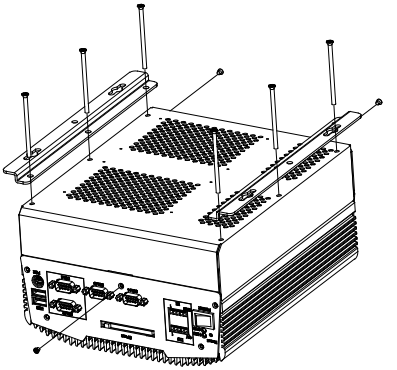
| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD | 2 | RXD |
| 3 | TXD | 4 | DTR |
| 5 | GND | 6 | DSR |
| 7 | RTS | 8 | CTS |
| 9 | RI | | |

### 2.4.8 USB Box Header (USB3~USB4)

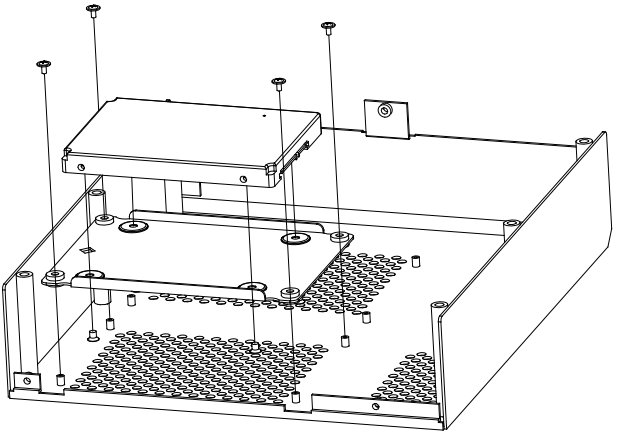
| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V | 2 | GND |
| 3 | USBD- | 4 | GND |
| 5 | USBD+ | 6 | USBD+ |
| 7 | GND | 8 | USBD- |
| 9 | GND | 10 | +5V |

## 2.5 HDD Installation

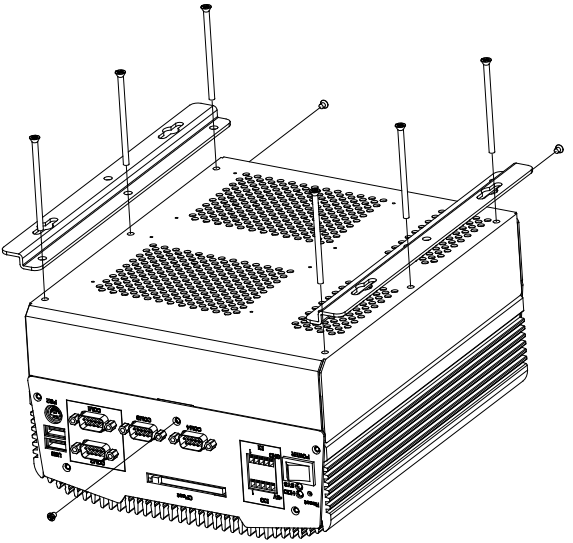
1. Unfasten the six screws on the bottom lid and three screws on the front and rear panel.



2. Place the HDD to the HDD bracket and fasten the four screws to the bottom lid of the AEC-6977.

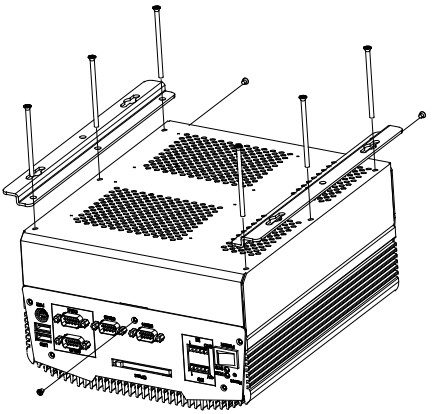


3. Fasten the screws on the front and rear panels, and the brackets of AEC-6977.

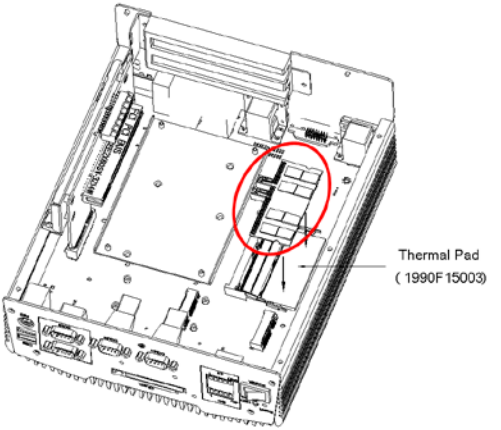


## 2.6 Memory Card Installation

1. Unfasten the six screws on the bottom lid and three screws on the front and rear panel.

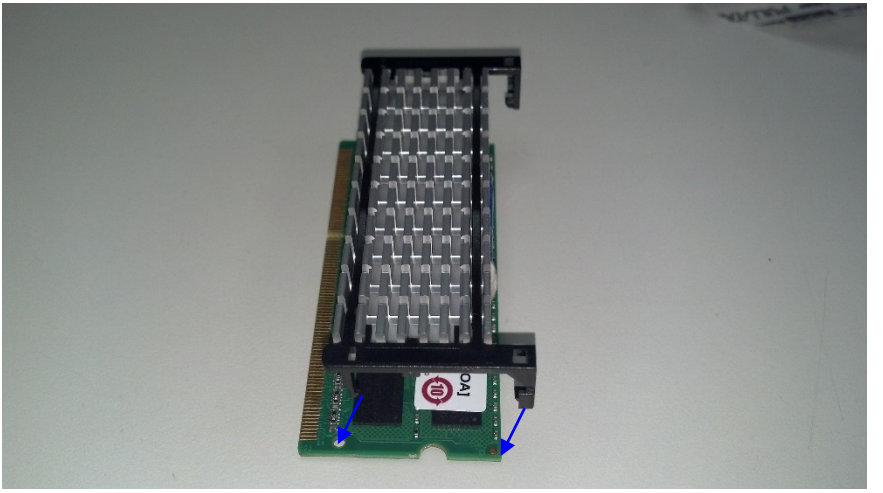


2. Insert the thermal pad to the memory slot first.

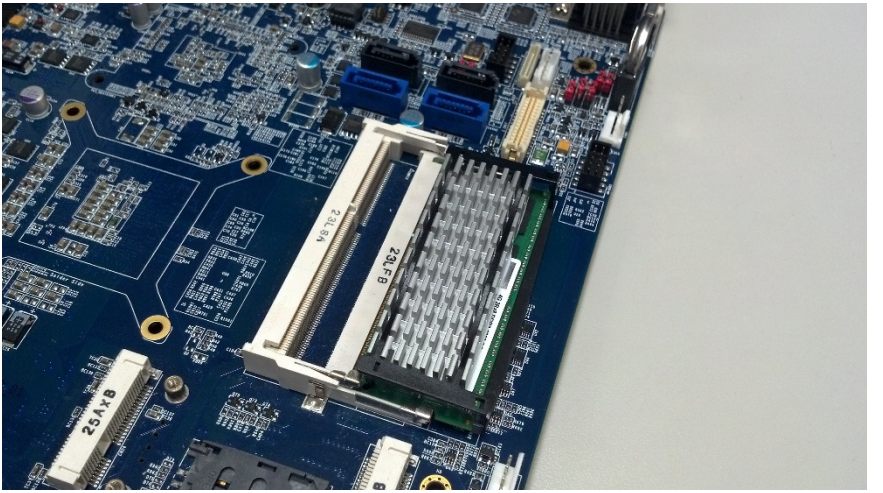


3. Remove the Release Paper (Liner) from the Heatsink module.

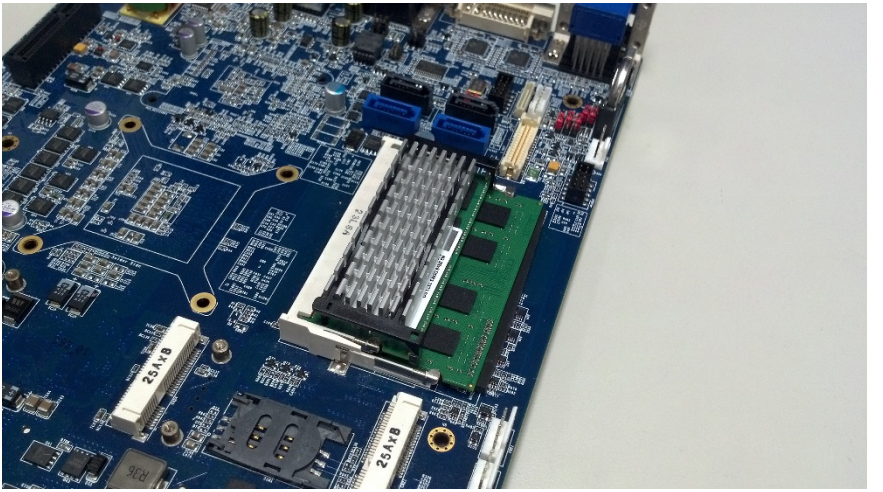

4. Line up the left leg of the Heatsink module with the round hole on the RAM card and the right leg with the edge of the RAM card as the following graphic shows. Then combine the Heatsink with the RAM card.



5. Insert the combined RAM module to the mainboard.

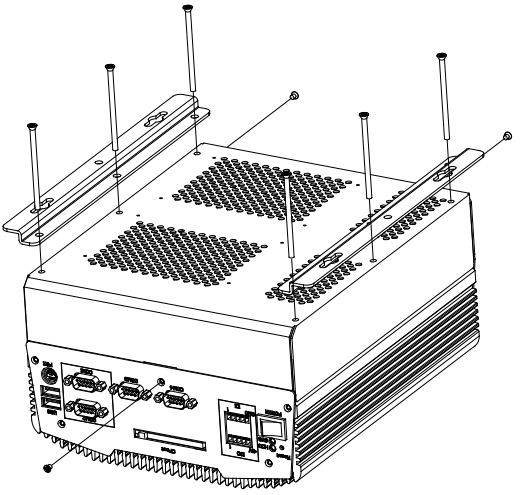


(Single RAM)



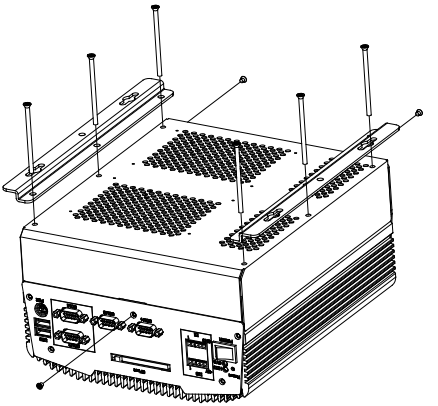
(Dual RAM)

6. Fasten the screws on the front and rear panels, and the brackets of AEC-6977.

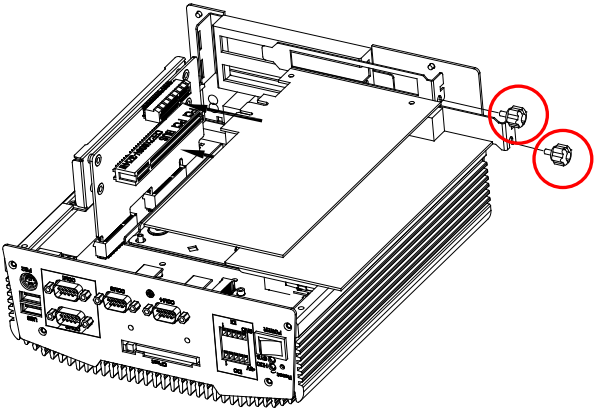


## 2.7 PCI Card Installation

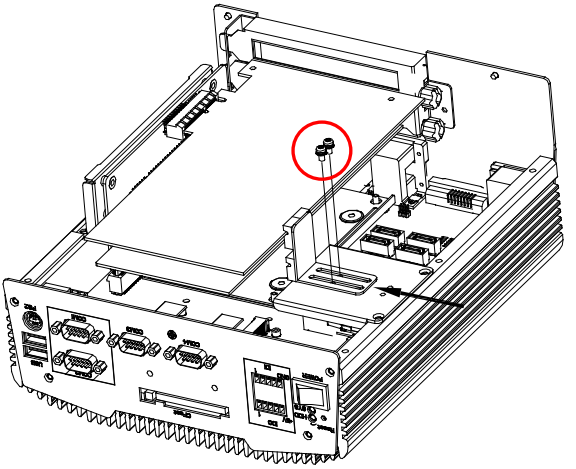
1. Unfasten the six screws on the bottom lid and three screws on the front and rear panel.



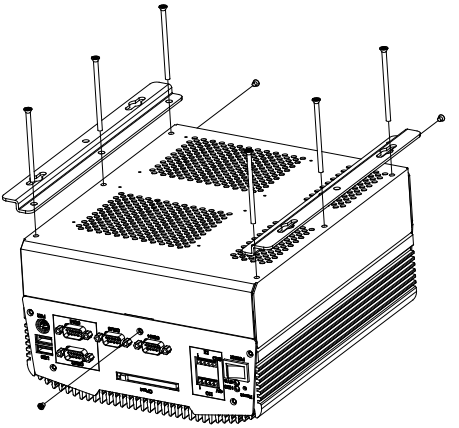
2. Insert the PCI bracket and fasten the two screws to fix the PCI bracket.



3. Install a hold-down bracket to fix the PCI Card and make sure the PCI Card installs properly. Then, use two screws to fix the hold-down bracket.

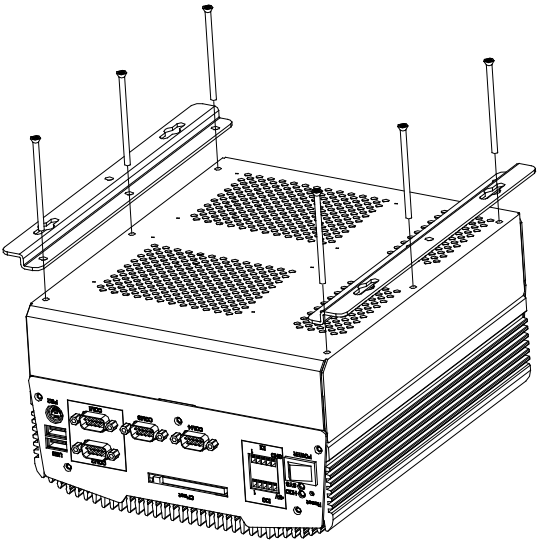


4. Fasten the screws on the front and rear panels, and the brackets of AEC-6977.



## 2.8 Wallmount Bracket Installation

Fasten the brackets with the appropriate screws.



# Chapter 3

AMI BIOS Setup

## 3.1 System Test and Initialization

The system uses certain routines to perform testing and initialization. If an error, fatal or non-fatal, is encountered, a few short beeps or an error message will be outputted. The board can usually continue the boot up sequence with non-fatal errors.

The system configuration verification routines check the current system configuration against the values stored in the CMOS memory. If they do not match, an error message will be outputted, in which case you will need to run the BIOS setup program to set the configuration information in memory.

There are three situations in which you will need to change the CMOS settings:

- You are starting your system for the first time
- You have changed your system's hardware
- The CMOS memory has lost power and the configuration information is erased

The system's CMOS memory uses a backup battery for data retention, which is to be replaced once emptied.

## 3.2 AMI BIOS Setup

The AMI BIOS ROM has a pre-installed Setup program that allows users to modify basic system configurations, which is stored in the battery-backed CMOS RAM and BIOS NVRAM so that the information is retained when the power is turned off.

To enter BIOS Setup, press <Del> or <F2> immediately while your computer is powering up.

The function for each interface can be found below.

**Main** – Date and time can be set here. Press <Tab> to switch between date elements

**Advanced** – Enable/ Disable boot option for legacy network devices

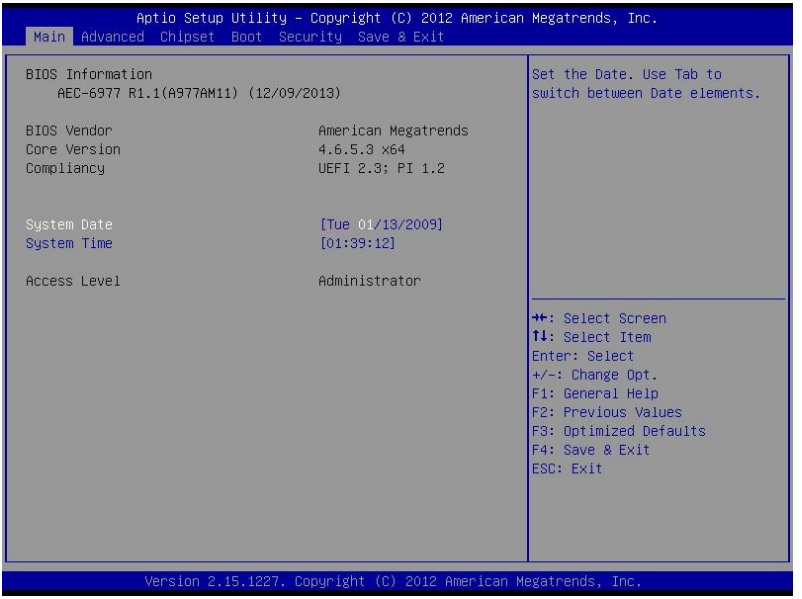
**Chipset** – For hosting bridge parameters

**Boot** – Enable/ Disable quiet Boot Option

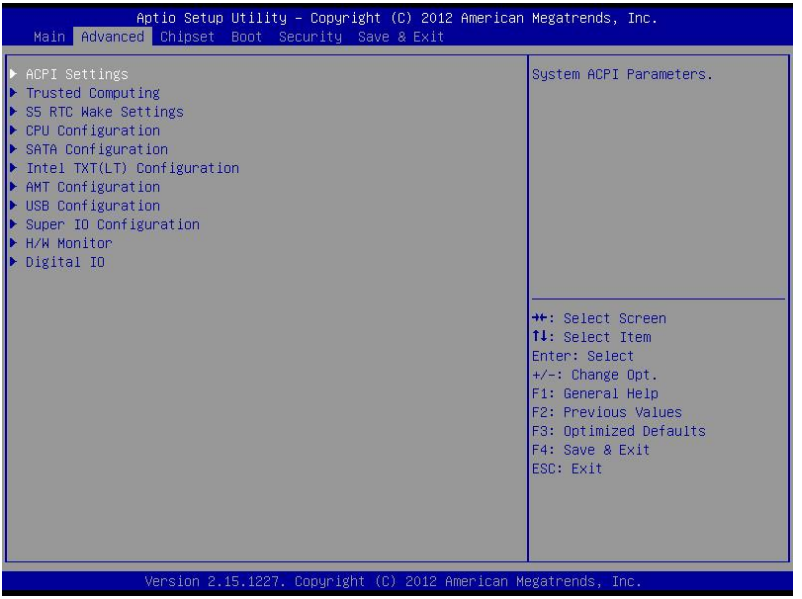
**Security** – The setup administrator password can be set here

**Save & Exit –**Save your changes and exit the program

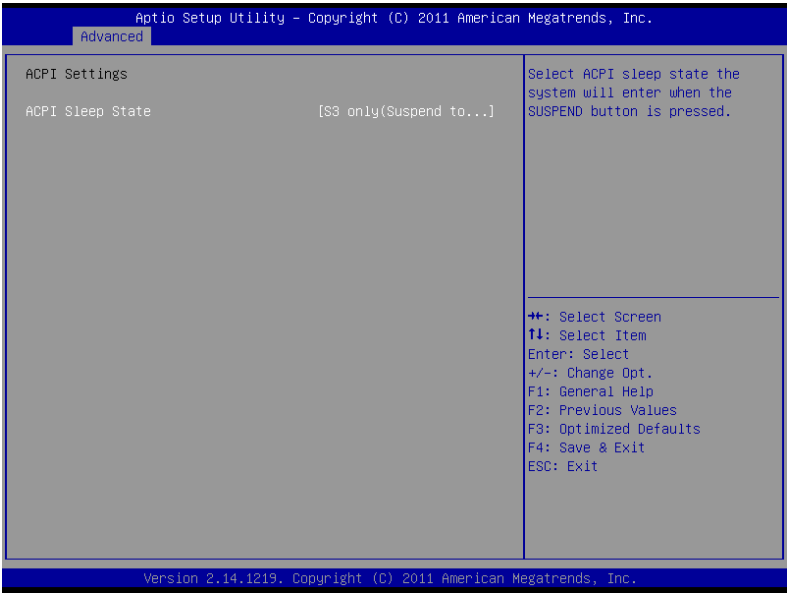
## 3.3 Setup Submenu: Main



## 3.4 Setup Submenu: Advanced



### 3.4.1 ACPI Settings




Options summary:

| | | |
|---|---|---|
| Suspend mode | Suspend Disabled | |
| | S1 only (CPU Stop Clock) | |
| | S3 only (Suspend to RAM) | Optimal Default, Failsafe Default |
| Select the ACPI state used for System Suspend | | |

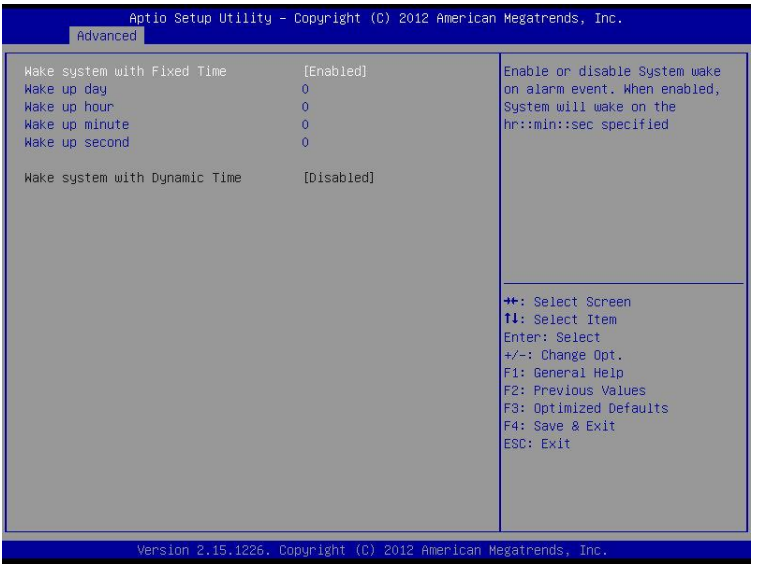
## 3.4.2 Advanced: Trusted Computing


Options summary:

| | | |
|---|---|---|
| Security Device Support | Disable | Optimal Default, Failsafe Default |
| | Enable | |
| Enables or Disabled BIOS support for security device. | | |

## 3.4.3 Advanced: S5 RTC Wake Settings (Fixed Time)

### 3.4.3.1 S5 RTC Wake Settings: Wake system with Fixed Time




Options summary:

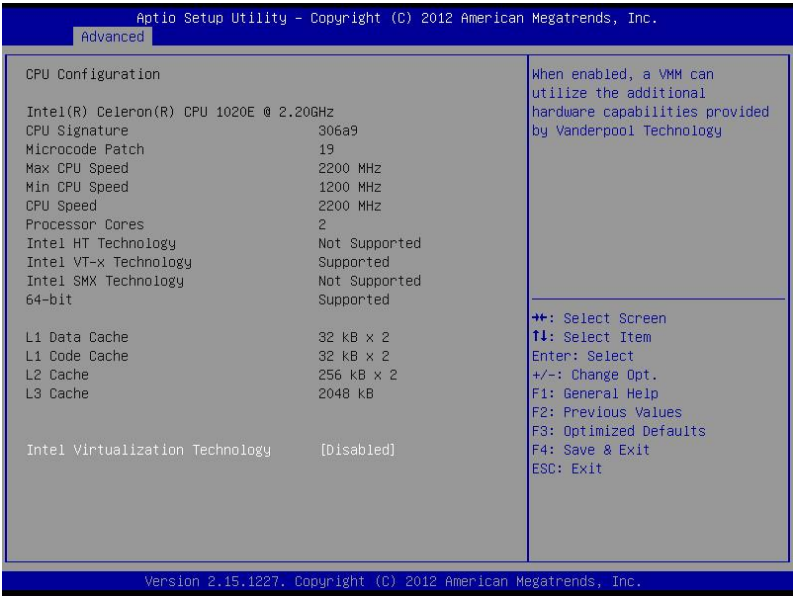
| | | |
|---|---|---|
| Wake system with Fixed Time | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| En/Disable System wake on alarm event. When enabled, System will wake on the hr:min:sec specified | | |
| Wake up day | 0-31 | Default 0 |
| Select 0 for daily system wake up, 1-31 for witch day of the moth that you would like the system to wake up. | | |
| Wake up day | 0-23 | Default 0 |
| Select 0-23 For example enter 3 for 3am and 15 for 3pm | | |
| Wake up day | 0-59 | Default 0 |
| Select 0-59 | | |
| Wake up day | 0-59 | Default 0 |
| Select 0-59 | | |

### 3.4.3.2 S5 RTC Wake Settings: Wake system with Dynamic Time


Options summary:

| | | |
|---|---|---|
| Wake system with Dynamic Time | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| En/Disable System wake on alarm event. When enabled, System will wake on current time + Increases minutese(s) | | |
| Wake up day | 1-5 | Default 1 |
| Select 1-5 | | |

### 3.4.4 Advanced: CPU Configuration

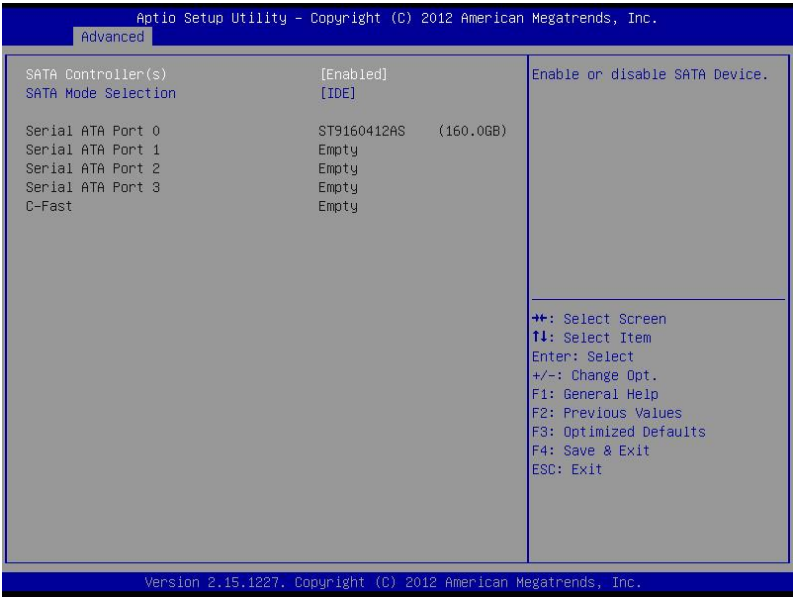



Options summary:

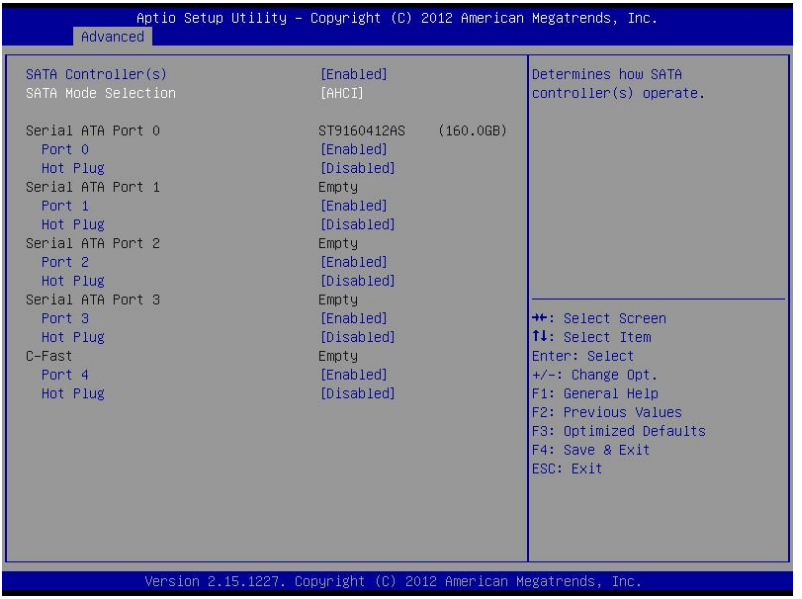
| | | |
|---|---|---|
| Intel Virtualization Technology | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology | | |

## 3.4.5 Advanced: SATA Configuration

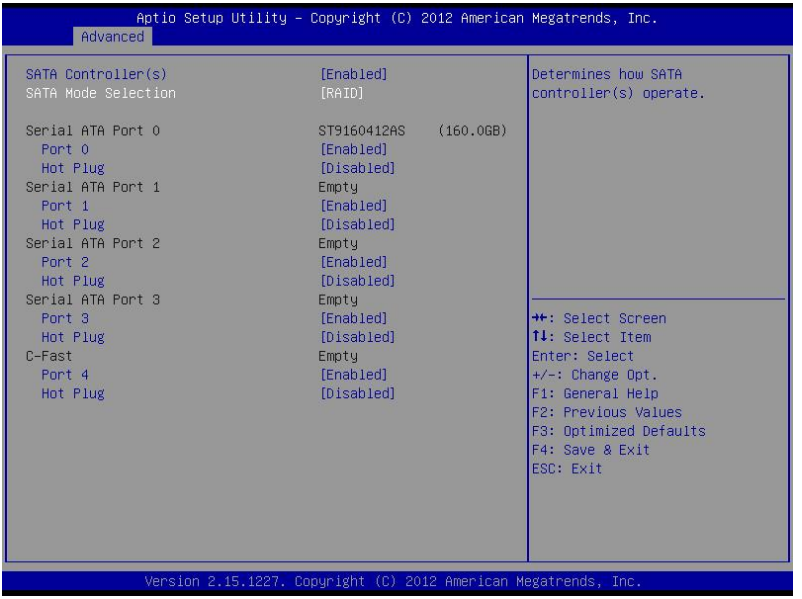
### 3.4.5.1 SATA Configuration: IDE



### 3.4.5.2 SATA Configuration: AHCI



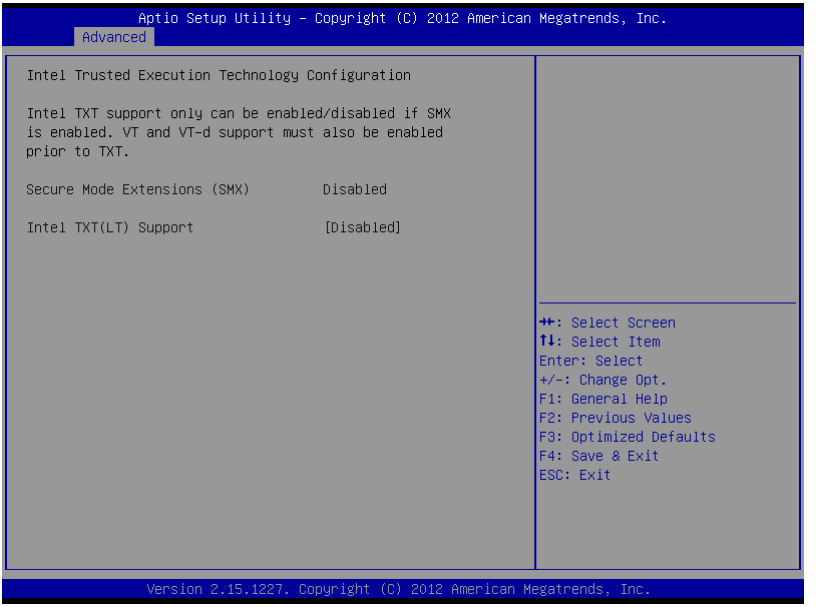
### 3.4.5.3 SATA Configuration: RAID



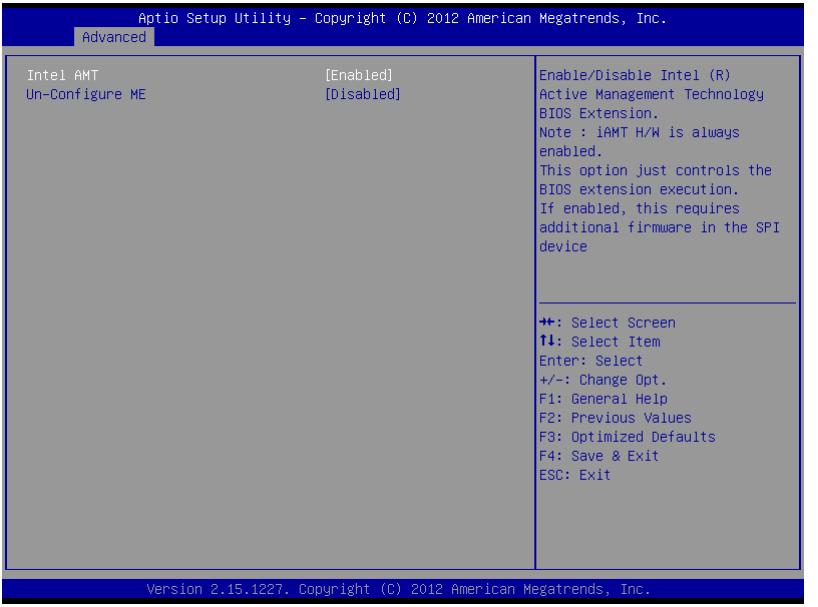

Options summary:

| | | |
|---|---|---|
| SATA Controllers | Disabled | |
| | Enabled | Default |
| En/Disable SATA Controller. | | |
| SATA Mode | IDE | Default |
| | AHCI | |
| | RAID | |
| IDE: Configure SATA controllers as legacy IDEAHCI: Configure SATA controllers to operate in AHCI mode | | |
| Port x | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| En/Disable SATA Port. | | |
| Hot Plug | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| En/Disable Hot Plug feature. | | |

## 3.4.6 Intel TXT(LT) Configuration



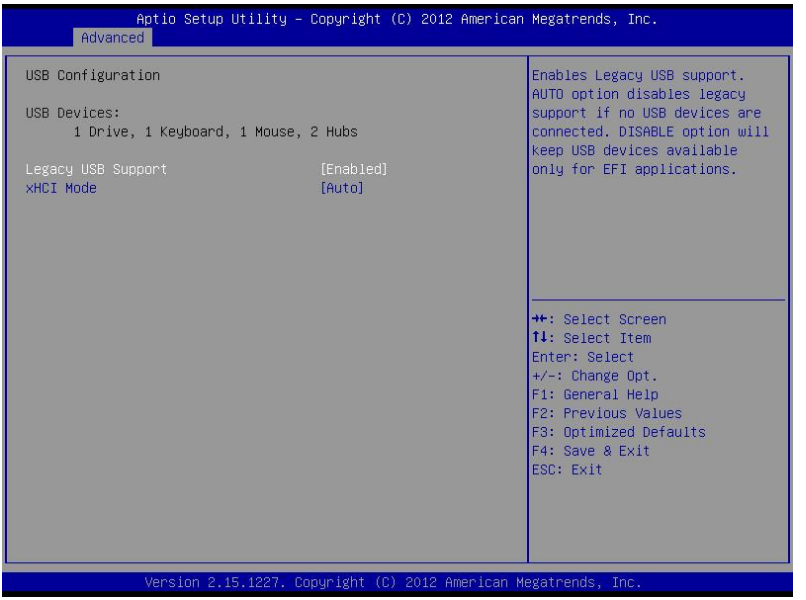
## 3.4.7 Advanced: AMT Configuration




Options summary:

| | | |
|---|---|---|
| Intel AMT | Disabled | |
| | Enabled | Optimal Default, Failsafe Default |
| En/Disable Intel Active Management Technology BIOS Extension. Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device. | | |
| Un-configure ME | Disabled | Optimal Default, Failsafe Default |
| | Enabled | |
| OEMFlag Bit 15: Un-Configure ME without password. | | |

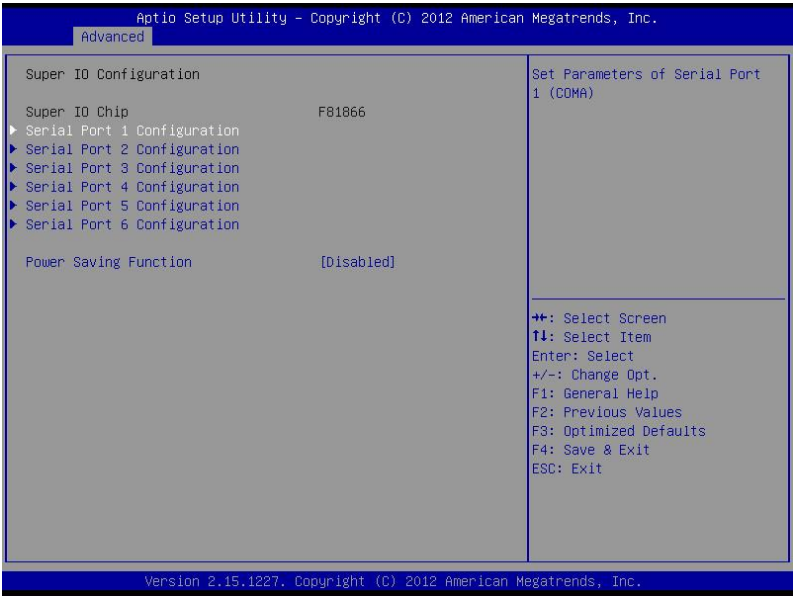
## 3.4.8 USB Configuration




Options summary:

| | | |
|---|---|---|
| Legacy USB Support | Enabled | Optimal Default, Failsafe Default |
| | Disabled | |
| | Auto | |
| Enables BIOS Support for Legacy USB Support. When enabled, USB can be functional in legacy environment like DOS.<br>AUTO option disables legacy support if no USB devices are connected | | |
| xHCI Mode | Smart Auto | Optimal Default, Failsafe Default |
| | Auto | |
| | Enabled | |
| | Disabled | |
| Mode of operation of xHCI controller | | |

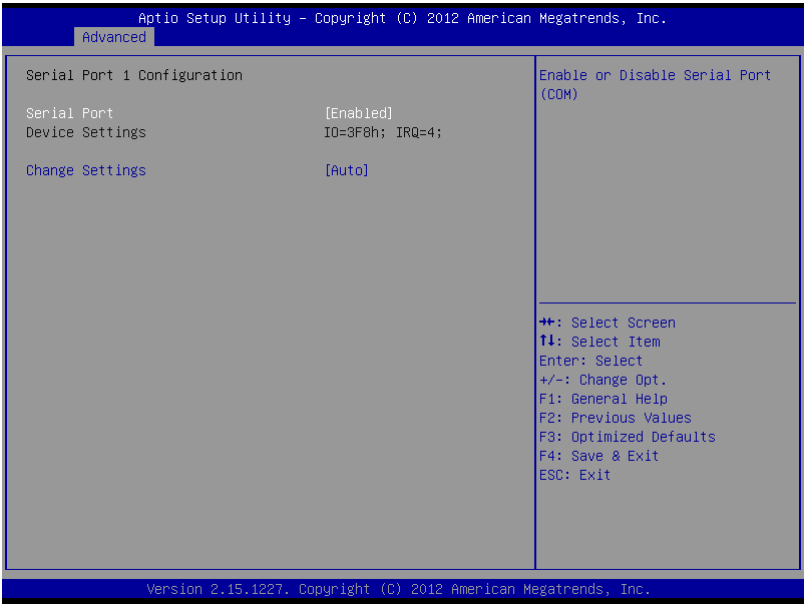
## 3.4.9 Advanced: Super IO Configuration




Options summary:

| | | |
|---|---|---|
| Power Saving Function | Disabled | Default |
| | Enabled | |
| Enable to reduce power consumption in system off state.<br>When Enabled, only power button can power-up system. | | |

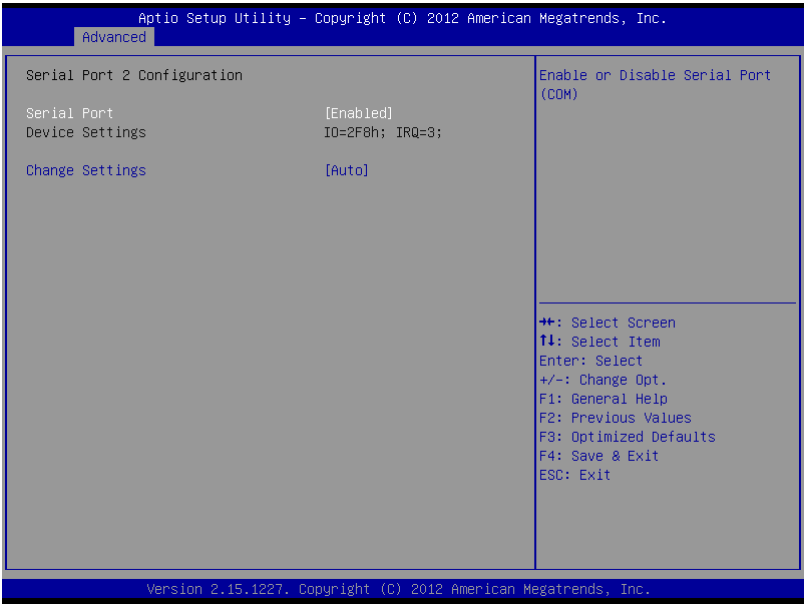
### 3.4.9.1 Super IO Configuration: Serial Port 1 Configuration




Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=3F8h; IRQ=4; | |
| | IO=3F8h; IRQ=3,4; | |
| | IO=2F8h; IRQ=3,4; | |
| | IO=3E8h; IRQ=3.4 | |
| | IO=2E8h; IRQ=3,4; | |
| Allows BIOS to Select Serial Port resource. | | |

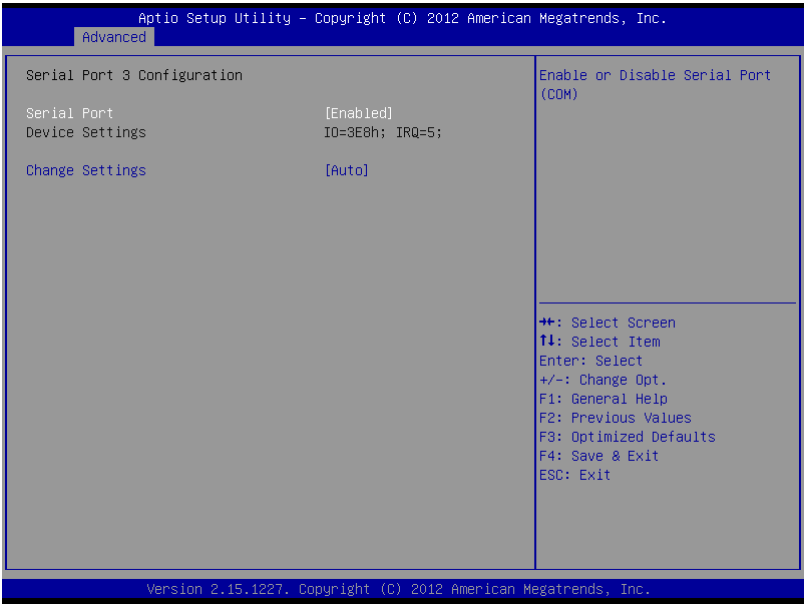
### 3.4.9.2 Super IO Configuration: Serial Port 2 Configuration




Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=2F8h; IRQ=3; | |
| | IO=3F8h; IRQ=3,4; | |
| | IO=2F8h; IRQ=3,4; | |
| | IO=3E8h; IRQ=3,4; | |
| | IO=2E8h; IRQ=3,4; | |
| Allows BIOS to Select Serial Port resource. | | |

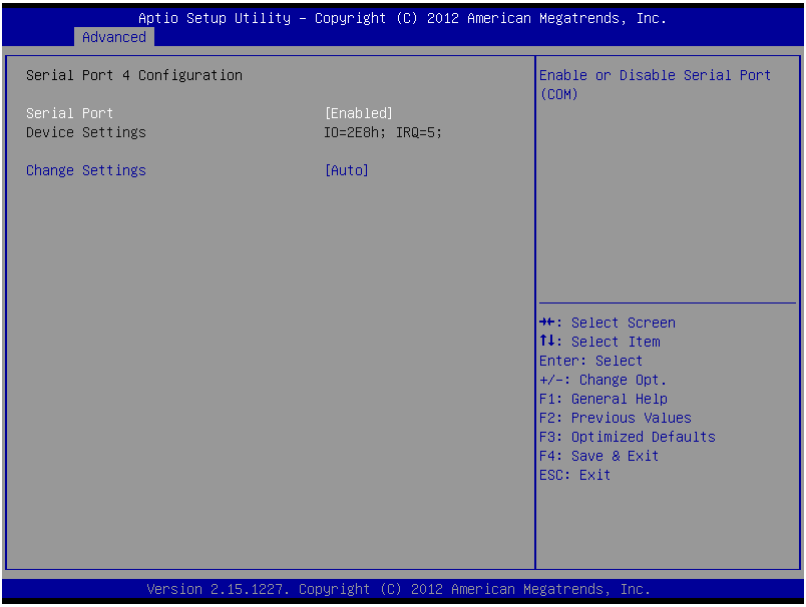
### 3.4.9.3 Super IO Configuration: Serial Port 3 Configuration




Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=3E8h; IRQ=10; | |
| | IO=3E8h; IRQ=10,11;; | |
| | IO=2E8h; IRQ=10,11; | |
| | IO=2D0h; IRQ=10,11; | |
| | IO=2D8h; IRQ=10,11; | |
| Allows BIOS to Select Serial Port resource. | | |

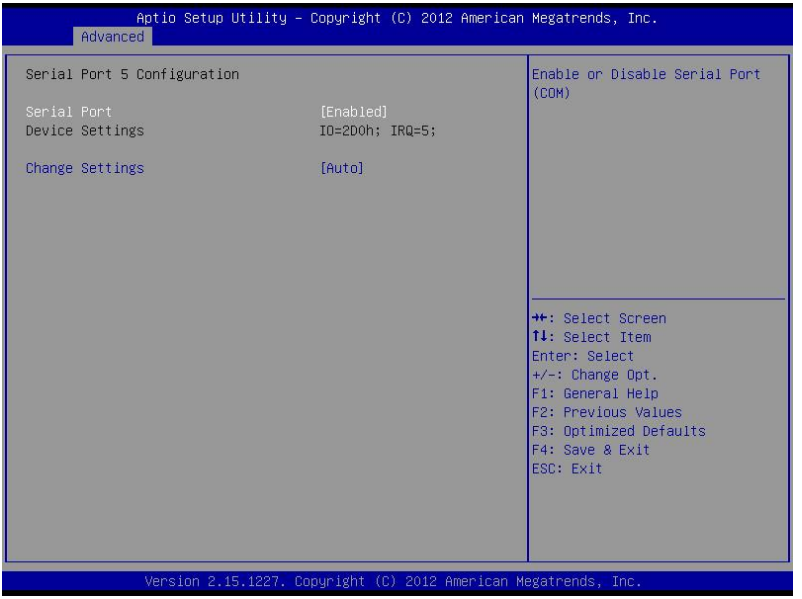
### 3.4.9.4 Super IO Configuration: Serial Port 4 Configuration




Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=2E8h; IRQ=10; | |
| | IO=3E8h; IRQ=10,11;; | |
| | IO=2E8h; IRQ=10,11; | |
| | IO=2D0h; IRQ=10,11; | |
| | IO=2D8h; IRQ=10,11; | |
| Allows BIOS to Select Serial Port resource. | | |

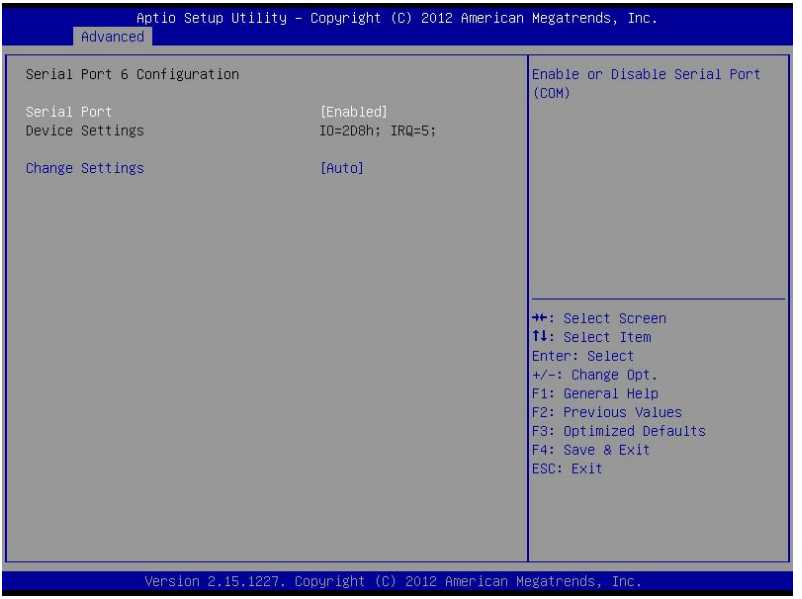
### 3.4.9.5 Super IO Configuration: Serial Port 5 Configuration




Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=2D0h; IRQ=5; | |
| | IO=3E8h; IRQ=5; | |
| | IO=2E8h; IRQ=5; | |
| | IO=2D0h; IRQ=5; | |
| Allows BIOS to Select Serial Port resource. | | |

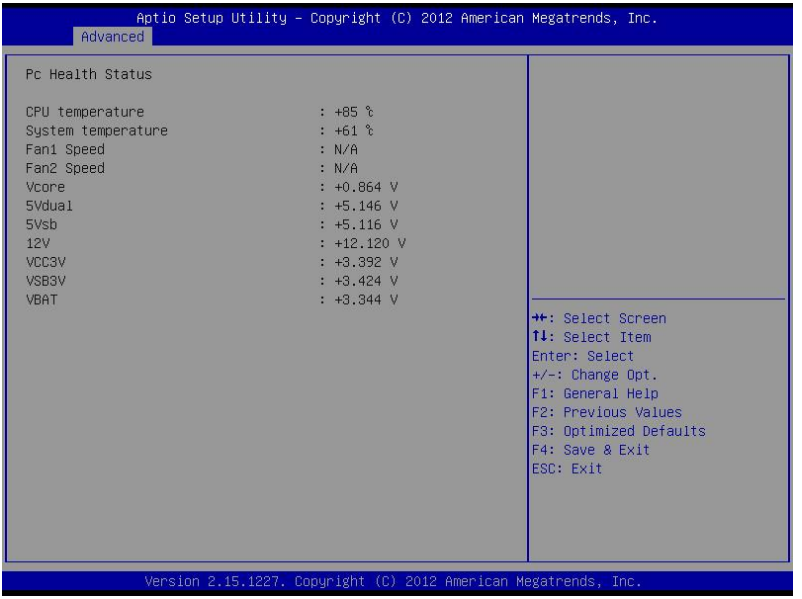
### 3.4.9.6 Super IO Configuration: Serial Port 6 Configuration



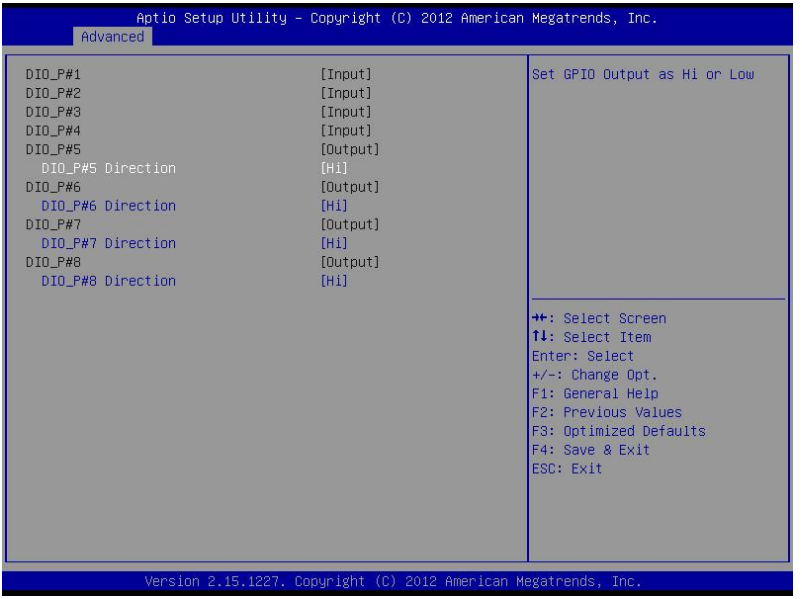

Options summary:

| | | |
|---|---|---|
| Serial Port | Disabled | |
| | Enabled | Default |
| Allows BIOS to En/Disable correspond serial port. | | |
| Change Settings | Auto | Default |
| | IO=2D8h; IRQ=5; | |
| | IO=3E8h; IRQ=5; | |
| | IO=2E8h; IRQ=5; | |
| | IO=2D0h; IRQ=5; | |
| Allows BIOS to Select Serial Port resource. | | |

### 3.4.10 Advanced: H/W Monitor



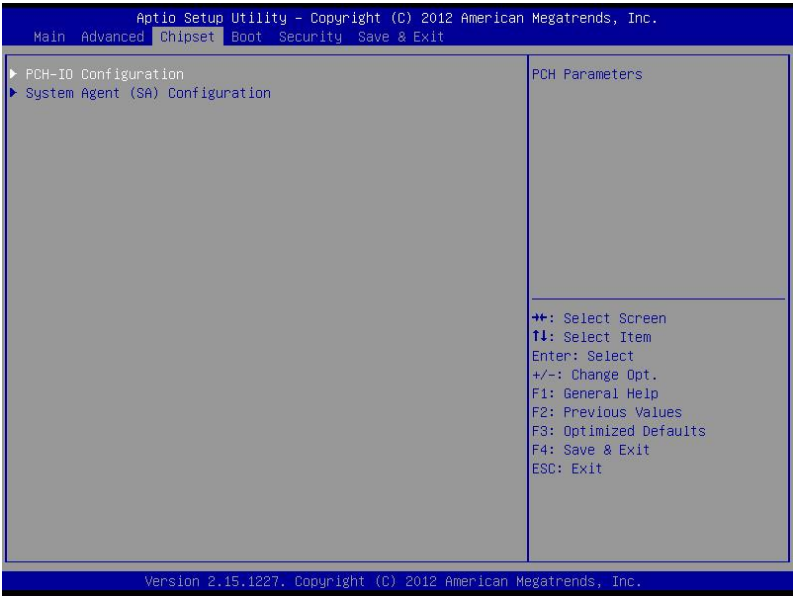
### 3.4.11 Advanced: Digital IO



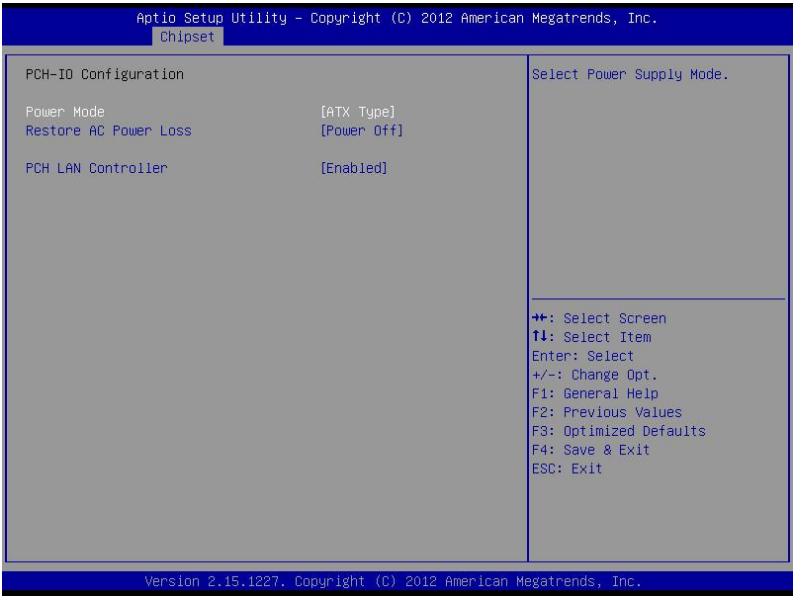

Options summary:

| | | |
|---|---|---|
| DIO_P#5~8 Direction | Low | |
| | Hi | Default |
| Allows BIOS to select high/low voltage level to output to corresponding DIO ping. | | |

## 3.5 Setup submenu: Chipset



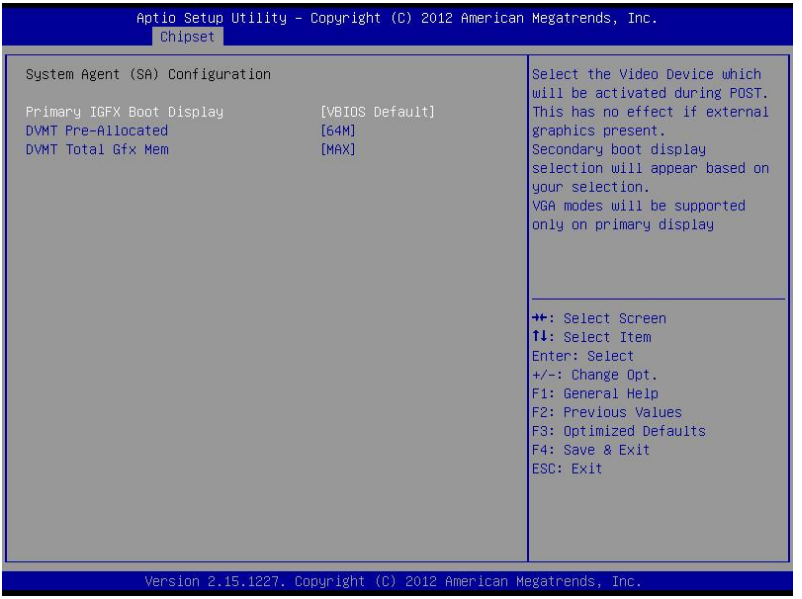
### 3.5.1 Chipset: PCH-IO Configuration




Options summary:

| | | |
|---|---|---|
| Power Mode | ATX Type | Default |
| | AT Type | |
| Select Power Supply Mode. | | |
| Power Mode | Power Off | Default |
| | Power On | |
| | Last State | |
| Select AC power state when power is re-applied after a power failure. | | |
| PCH LAN Controller | Enabled | Default |
| | Disabled | |
| Enable or disable onboard NIC. | | |

## 3.5.2 Chipset: System Agent (SA) Configuration




Options summary:

| | | |
|---|---|---|
| Primary IGFX Boot Display | VBIOS Default | Default |
| | CRT | |
| | HDMI | |
| | DVI | |
| Select the Video Device which will be activated during POST. | | |
| DVMT Pre-Allocated | 32M | |
| | 64M | Default |
| | 96M | |
| | 128M | |
| | 160M | |
| | 192M | |
| | 224M | |
| | 256M | |
| | 288M | |
| | 320M | |
| | 352M | |
| | 284M | |

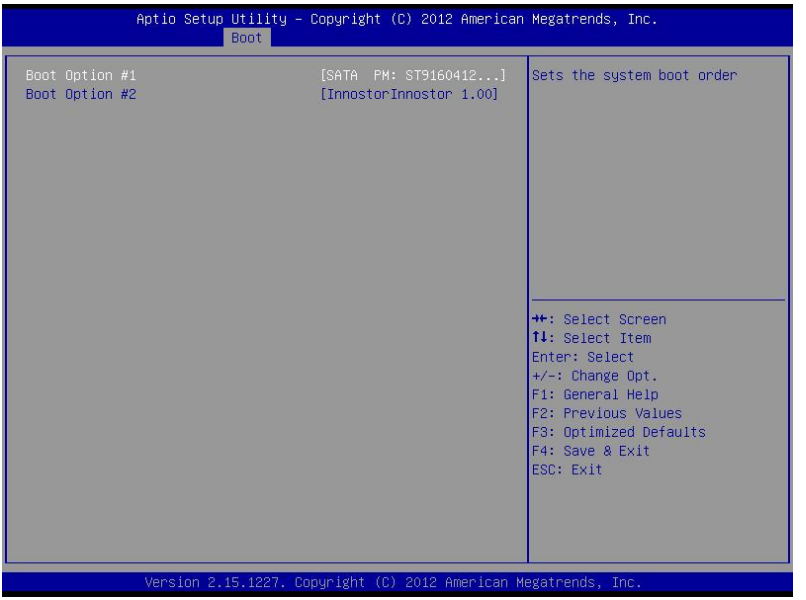
| | | |
|---|---|---|
| | 416M | |
| | 448M | |
| | 480M | |
| | 512M | |
| | 1024M | |
| Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device. | | |
| DVMT Total Gfx Mem | 128M | |
| | 256M | |
| | MAX | Default |
| Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device. | | |

## 3.6 Setup submenu: Boot

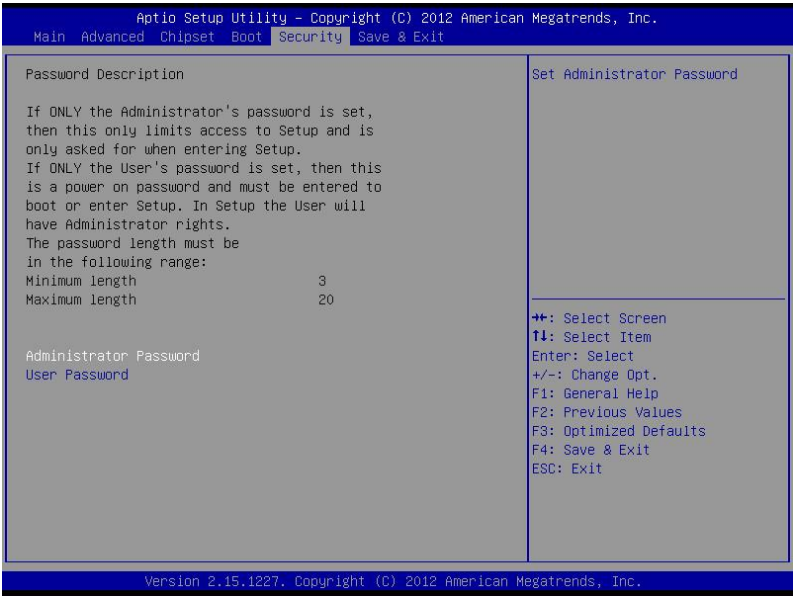

Options summary:

| | | |
|---|---|---|
| Quiet Boot | Disabled | |
| | Enabled | Default |
| En/Disable showing boot logo. | | |
| Launch I82579LM PXE OpROM | Disabled | Default |
| | Enabled | |
| En/Disable Legacy Boot Option for I82579LM. | | |
| Launch I82574L PXE OpROM | Disabled | Default |
| | Enabled | |
| En/Disable Legacy Boot Option for I82583V. | | |

### 3.6.1 Boot: BBS Priorities



## 3.7 Setup submenu: Security




### Change User/Administrator Password

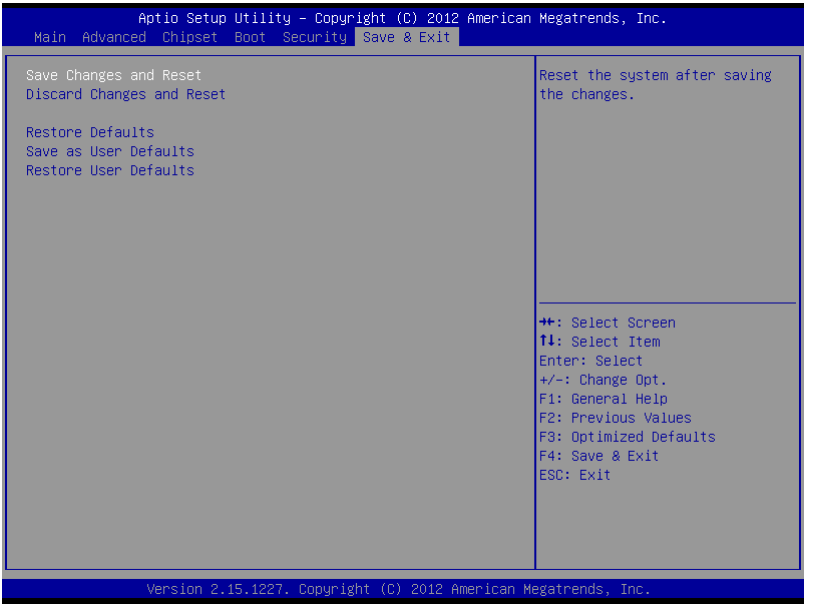
You can set a User Password once an Administrator Password is set. The password will be required during boot up, or when the user enters the Setup utility. Please Note that a User Password does not provide access to many of the features in the Setup utility.

Select the password you wish to set, press Enter to open a dialog box to enter your password (you can enter no more than six letters or numbers). Press Enter to confirm your entry, after which you will be prompted to retype your password for a final confirmation. Press Enter again after you have retyped it correctly.

### Removing the Password

Highlight this item and type in the current password. At the next dialog box press Enter to disable password protection.

## 3.8 Setup submenu: Save & Exit



# Chapter 4

Drivers Installation

## 4.1 Product CD/DVD

The AEC-6977 comes with a product DVD that contains all the drivers and utilities you need to setup your product. Insert the DVD and follow the steps in the autorun program to install the drivers.

In case the program does not start, follow the sequence below to install the drivers.

### Step 1 – Install Chipset Drivers

1. Open the **Step 1 - Chipset** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 2 – Install VGA Driver

1. Open the **Step 2 - VGA** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Note 1:

☐ This motherboard supports VGA and LVDS display devices. In Single Display mode, use the hot keys to switch between VGA to LVDS device or vice versa. By default, press <Ctrl>+<Alt>+<F1> to switch to VGA device and press <Ctrl>+<Alt>+<F3> to switch to LVDS device.

☐ Before removing the current display device, connect the display device that you want to use, and then press the hot keys to switch to that device.

Note 2:

If the OS is Windows® XP, you have to install the driver of dotNet Framework first.

Simply click on dotnetfx35.exe located in .Net Framwork folder.

### Step 3 – Install LAN Driver

1. Open the **Step 3 - LAN** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 4 – Install Audio Driver

1. Open the **Step 4 - Audio** folder and select your OS
2. Open the **.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

### Step 5 – Install USB 3.0 Driver (Windows 7 only)

1. Open the **Step 4 – USB 3.0** followed by the **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

### Step 6 – Install RAID & AHCI Drivers

Please refer to Appendix C RAID & AHCI Settings

### Step 7 – Install ME Drivers

1. Open the **Step 7 – ME** folder and followed by **Setup.exe** file
2. Follow the instructions
3. Drivers will be installed automatically

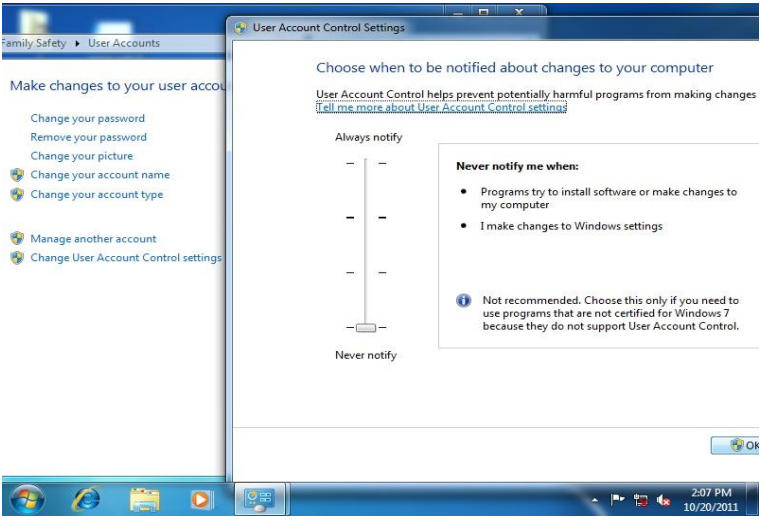
## Step 8 – Install TPM Driver

1. Open the **Step 8 - TPM** folder and select your OS
2. Open the **Setup.exe** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

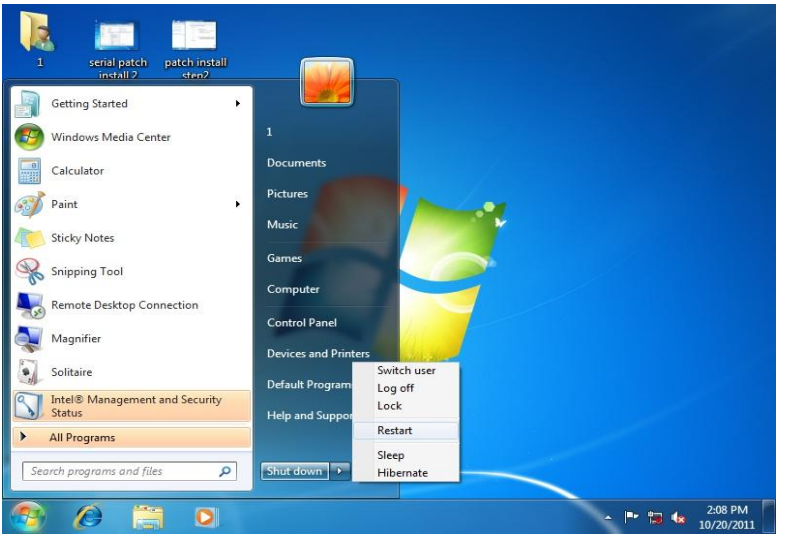
## Step 9 – Install Serial Port Driver (Optional)

For Windows 7:

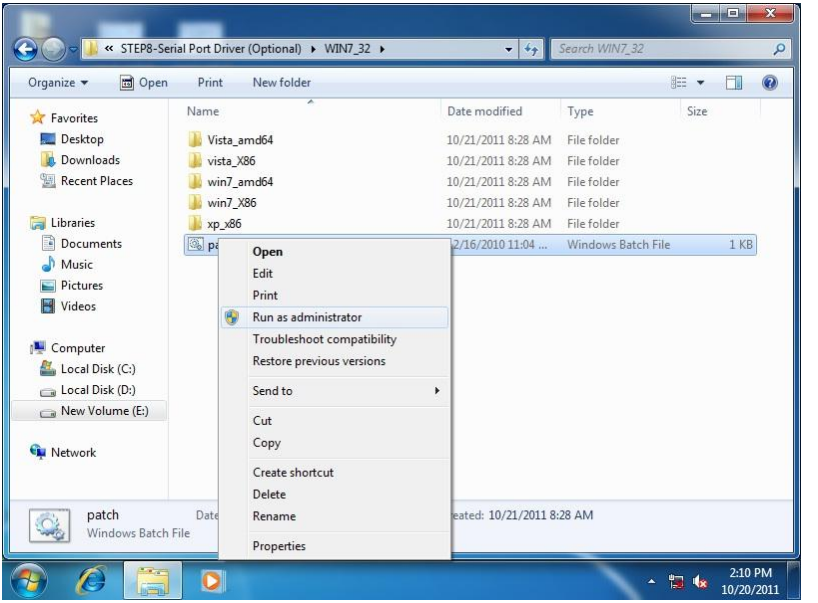
1. Change User Account Control settings to **Never notify**




2. Reboot and log in as administrator




3. Open the **Step 9 - Serial Port Driver (Optional)** folder and run **patch.bat** as administrator



For Windows 8 and Windows 10:

1. Open the **Step 9 - Serial Port Driver (Optional)** folder and select your OS
2. Open the **patch.bat** file in the folder
3. Follow the instructions
4. Drivers will be installed automatically

# Appendix A

Watchdog Timer Programming

## A.1 Watchdog Timer Initial Program

| Table 1 : SuperIO relative register table | | |
|---|---|---|
| | Default Value | Note |
| Index | 0x2E(Note1) | SIO MB PnP Mode Index Register<br>0x2E or 0x4E |
| Data | 0x2F(Note2) | SIO MB PnP Mode Data Register<br>0x2F or 0x4F |

| Table 2 : Watchdog relative register table | | | | | |
|---|---|---|---|---|---|
| | LDN | Register | BitNum | Value | Note |
| Timer Counter | 0x07(Note3) | 0xF6(Note4) | | (Note24) | Time of watchdog timer (0~255)<br>This register is byte access |
| Counting Unit | 0x07(Note5) | 0xF5(Note6) | 3(Note7) | 0(Note8) | Select time unit.<br>0: second<br>1: minute |
| Watchdog Enable | 0x07(Note9) | 0xF5(Note10) | 5(Note11) | 1(Note12) | 0: Disable<br>1: Enable |
| Timeout Status | 0x07(Note13) | 0xF5(Note14) | 6(Note15) | 1 | 1: Clear timeout status |
| Output Mode | 0x07(Note16) | 0xF5(Note17) | 4(Note18) | 1(Note19) | Select WDTRST# output mode<br>0: level<br>1: pulse |
| WDTRST output | 0x07(Note20) | 0xFA(Note21) | 0(Note22) | 1(Note23) | Enable/Disable time out output via WDTRST#<br>0: Disable<br>1: Enable |

## A.2 Watchdog Sample Program

```
//******************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData   //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Watch Dog relative definition (Please reference to Table 2)
#define byte   TimerLDN   //This parameter is represented from Note3
#define byte   TimerReg   //This parameter is represented from Note4
#define byte   TimerVal   // This parameter is represented from Note24
#define byte   UnitLDN   //This parameter is represented from Note5
#define byte   UnitReg   //This parameter is represented from Note6
#define byte   UnitBit   //This parameter is represented from Note7
#define byte   UnitVal   //This parameter is represented from Note8
#define byte   EnableLDN   //This parameter is represented from Note9
#define byte   EnableReg   //This parameter is represented from Note10
#define byte   EnableBit   //This parameter is represented from Note11
#define byte   EnableVal   //This parameter is represented from Note12
#define byte   StatusLDN   // This parameter is represented from Note13
#define byte   StatusReg   // This parameter is represented from Note14
#define byte   StatusBit   // This parameter is represented from Note15
#define byte   ModeLDN   // This parameter is represented from Note16
#define byte   ModeReg   // This parameter is represented from Note17
#define byte   ModeBit   // This parameter is represented from Note18
#define byte   ModeVal   // This parameter is represented from Note19
#define byte   WDTRstLDN   // This parameter is represented from Note20
#define byte   WDTRstReg   // This parameter is represented from Note21
#define byte   WDTRstBit   // This parameter is represented from Note22
#define byte   WDTRstVal   // This parameter is represented from Note23
//******************************************************************************
```

```
*********************************************************************************
VOID    Main(){
        // Procedure : AaeonWDTConfig
        // (byte)Timer : Time of WDT timer.(0x00~0xFF)
        // (boolean)Unit : Select time unit(0: second, 1: minute).
        AaeonWDTConfig();

        // Procedure : AaeonWDTEnable
         // This procudure will enable the WDT counting.
        AaeonWDTEnable();
}
*********************************************************************************
```

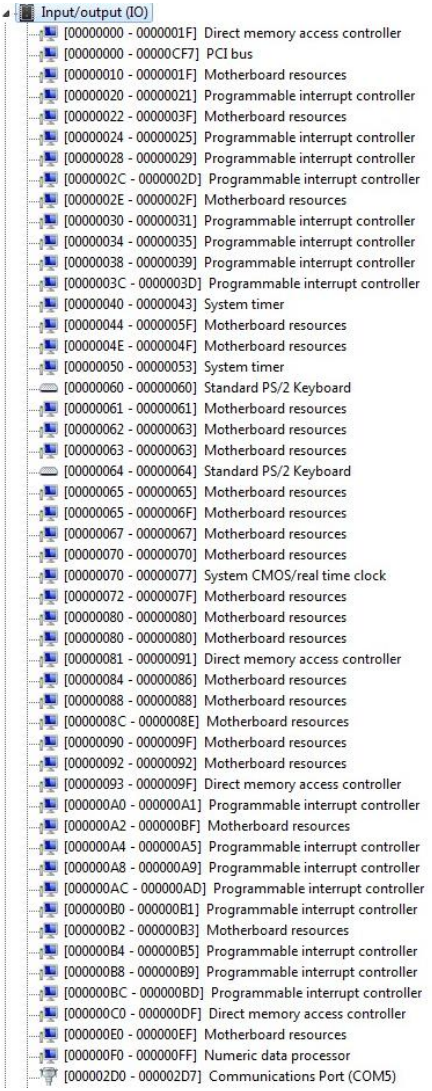
```
*******************************************************************************
// Procedure : AaeonWDTEnable
VOID    AaeonWDTEnable (){
        WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 1);
}

// Procedure : AaeonWDTConfig
VOID    AaeonWDTConfig (){
         // Disable WDT counting
         WDTEnableDisable(EnableLDN, EnableReg, EnableBit, 0);
         // Clear Watchdog Timeout Status
         WDTClearTimeoutStatus();
         // WDT relative parameter setting
         WDTParameterSetting();
}

VOID    WDTEnableDisable(byte LDN, byte Register, byte BitNum, byte Value){
        SIOBitSet(LDN, Register, BitNum, Value);
}

VOID    WDTParameterSetting(){
         // Watchdog Timer counter setting
        SIOByteSet(TimerLDN, TimerReg, TimerVal);
       // WDT counting unit setting
       SIOBitSet(UnitLDN, UnitReg, UnitBit, UnitVal);
       // WDT output mode setting, level / pulse
       SIOBitSet(ModeLDN, ModeReg, ModeBit, ModeVal);
        // Watchdog timeout output via WDTRST#
        SIOBitSet(WDTRstLDN, WDTRstReg, WDTRstBit, WDTRstVal);
}

VOID    WDTClearTimeoutStatus(){
        SIOBitSet(StatusLDN, StatusReg, StatusBit, 1);
}
*******************************************************************************
```

```
*****************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*****************************************************************************
```

# Appendix B

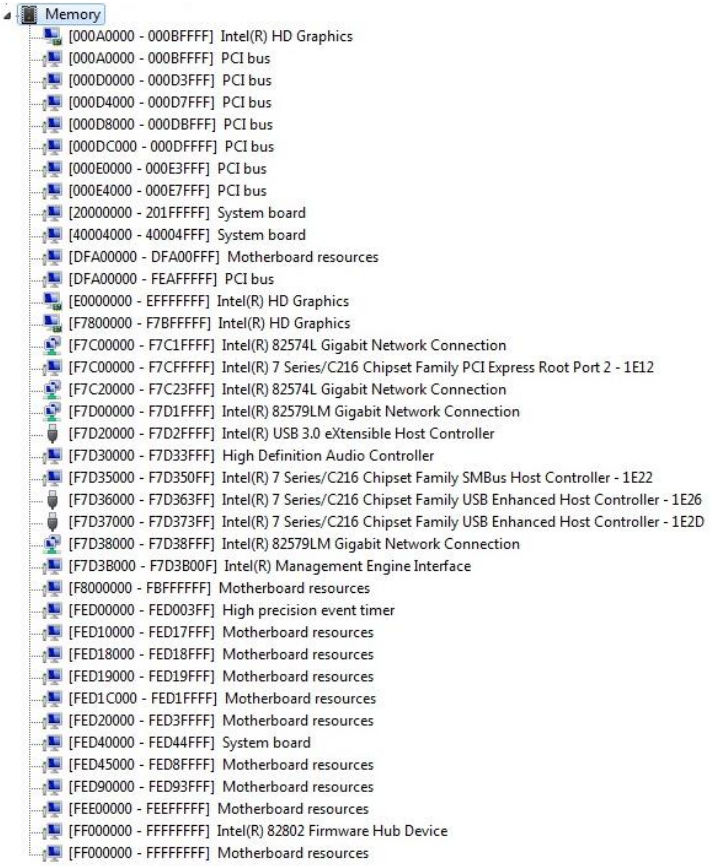
I/O Information

## B.1 I/O Address Map

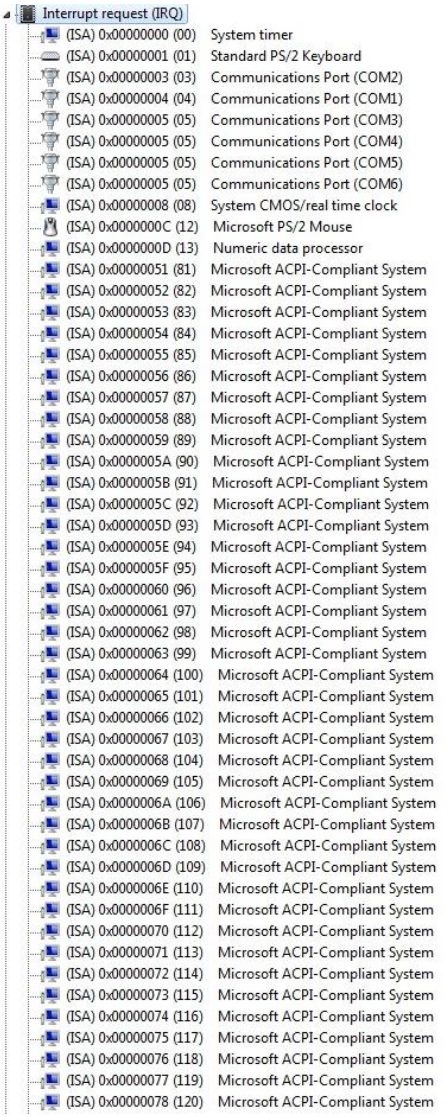


- [000002D8 - 000002DF] Communications Port (COM6)
- [000002E8 - 000002EF] Communications Port (COM4)
- [000002F8 - 000002FF] Communications Port (COM2)
- [000003B0 - 000003BB] Intel(R) HD Graphics
- [000003C0 - 000003DF] Intel(R) HD Graphics
- [000003E8 - 000003EF] Communications Port (COM3)
- [000003F8 - 000003FF] Communications Port (COM1)
- [00000400 - 00000453] Motherboard resources
- [00000454 - 00000457] Motherboard resources
- [00000458 - 0000047F] Motherboard resources
- [000004D0 - 000004D1] Motherboard resources
- [000004D0 - 000004D1] Programmable interrupt controller
- [00000500 - 0000057F] Motherboard resources
- [00000680 - 0000069F] Motherboard resources
- [00000A00 - 00000A0F] Motherboard resources
- [00000A10 - 00000A1F] Motherboard resources
- [00000A20 - 00000A2F] Motherboard resources
- [00000D00 - 0000FFFF] PCI bus
- [00001000 - 0000100F] Motherboard resources
- [0000164E - 0000164F] Motherboard resources
- [0000E000 - 0000EFFF] Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
- [0000F000 - 0000F03F] Intel(R) HD Graphics
- [0000F040 - 0000F05F] Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
- [0000F080 - 0000F08F] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F090 - 0000F09F] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F0A0 - 0000F0A3] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F0B0 - 0000F0B7] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F0C0 - 0000F0C3] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F0D0 - 0000F0D7] Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
- [0000F0E0 - 0000F0EF] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000F0F0 - 0000F0FF] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000F100 - 0000F103] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000F110 - 0000F117] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000F120 - 0000F123] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000F130 - 0000F137] Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
- [0000FFFF - 0000FFFF] Motherboard resources
- [0000FFFF - 0000FFFF] Motherboard resources

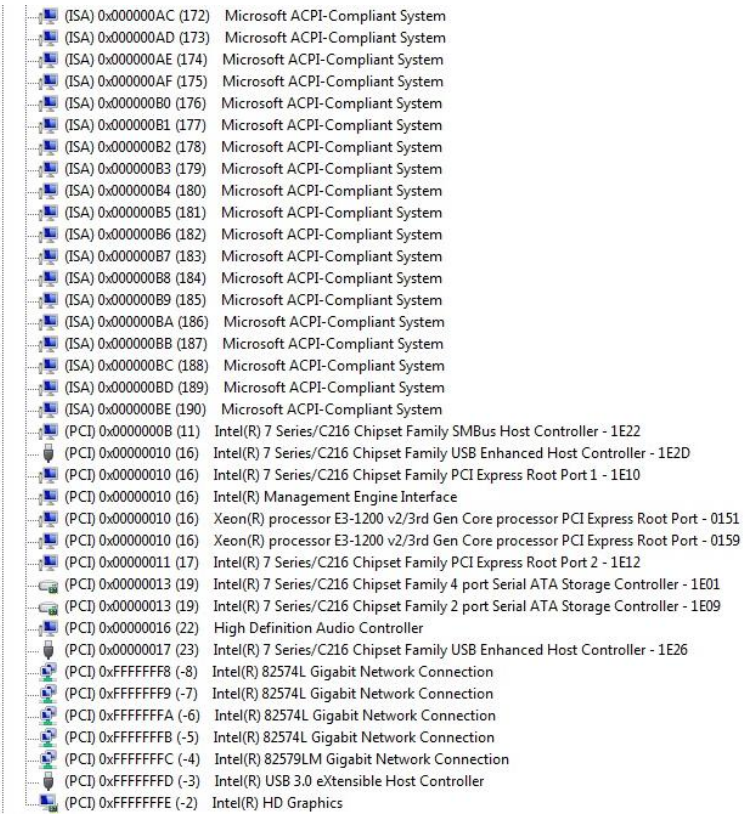
## B.2 Memory Address Map



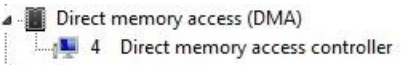
## B.3 IRQ Mapping Chart



- (ISA) 0x00000079 (121) Microsoft ACPI-Compliant System
- (ISA) 0x0000007A (122) Microsoft ACPI-Compliant System
- (ISA) 0x0000007B (123) Microsoft ACPI-Compliant System
- (ISA) 0x0000007C (124) Microsoft ACPI-Compliant System
- (ISA) 0x0000007D (125) Microsoft ACPI-Compliant System
- (ISA) 0x0000007E (126) Microsoft ACPI-Compliant System
- (ISA) 0x0000007F (127) Microsoft ACPI-Compliant System
- (ISA) 0x00000080 (128) Microsoft ACPI-Compliant System
- (ISA) 0x00000081 (129) Microsoft ACPI-Compliant System
- (ISA) 0x00000082 (130) Microsoft ACPI-Compliant System
- (ISA) 0x00000083 (131) Microsoft ACPI-Compliant System
- (ISA) 0x00000084 (132) Microsoft ACPI-Compliant System
- (ISA) 0x00000085 (133) Microsoft ACPI-Compliant System
- (ISA) 0x00000086 (134) Microsoft ACPI-Compliant System
- (ISA) 0x00000087 (135) Microsoft ACPI-Compliant System
- (ISA) 0x00000088 (136) Microsoft ACPI-Compliant System
- (ISA) 0x00000089 (137) Microsoft ACPI-Compliant System
- (ISA) 0x0000008A (138) Microsoft ACPI-Compliant System
- (ISA) 0x0000008B (139) Microsoft ACPI-Compliant System
- (ISA) 0x0000008C (140) Microsoft ACPI-Compliant System
- (ISA) 0x0000008D (141) Microsoft ACPI-Compliant System
- (ISA) 0x0000008E (142) Microsoft ACPI-Compliant System
- (ISA) 0x0000008F (143) Microsoft ACPI-Compliant System
- (ISA) 0x00000090 (144) Microsoft ACPI-Compliant System
- (ISA) 0x00000091 (145) Microsoft ACPI-Compliant System
- (ISA) 0x00000092 (146) Microsoft ACPI-Compliant System
- (ISA) 0x00000093 (147) Microsoft ACPI-Compliant System
- (ISA) 0x00000094 (148) Microsoft ACPI-Compliant System
- (ISA) 0x00000095 (149) Microsoft ACPI-Compliant System
- (ISA) 0x00000096 (150) Microsoft ACPI-Compliant System
- (ISA) 0x00000097 (151) Microsoft ACPI-Compliant System
- (ISA) 0x00000098 (152) Microsoft ACPI-Compliant System
- (ISA) 0x00000099 (153) Microsoft ACPI-Compliant System
- (ISA) 0x0000009A (154) Microsoft ACPI-Compliant System
- (ISA) 0x0000009B (155) Microsoft ACPI-Compliant System
- (ISA) 0x0000009C (156) Microsoft ACPI-Compliant System
- (ISA) 0x0000009D (157) Microsoft ACPI-Compliant System
- (ISA) 0x0000009E (158) Microsoft ACPI-Compliant System
- (ISA) 0x0000009F (159) Microsoft ACPI-Compliant System
- (ISA) 0x000000A0 (160) Microsoft ACPI-Compliant System
- (ISA) 0x000000A1 (161) Microsoft ACPI-Compliant System
- (ISA) 0x000000A2 (162) Microsoft ACPI-Compliant System
- (ISA) 0x000000A3 (163) Microsoft ACPI-Compliant System
- (ISA) 0x000000A4 (164) Microsoft ACPI-Compliant System
- (ISA) 0x000000A5 (165) Microsoft ACPI-Compliant System
- (ISA) 0x000000A6 (166) Microsoft ACPI-Compliant System
- (ISA) 0x000000A7 (167) Microsoft ACPI-Compliant System
- (ISA) 0x000000A8 (168) Microsoft ACPI-Compliant System
- (ISA) 0x000000A9 (169) Microsoft ACPI-Compliant System
- (ISA) 0x000000AA (170) Microsoft ACPI-Compliant System
- (ISA) 0x000000AB (171) Microsoft ACPI-Compliant System


(ISA) 0x000000AC (172) Microsoft ACPI-Compliant System
(ISA) 0x000000AD (173) Microsoft ACPI-Compliant System
(ISA) 0x000000AE (174) Microsoft ACPI-Compliant System
(ISA) 0x000000AF (175) Microsoft ACPI-Compliant System
(ISA) 0x000000B0 (176) Microsoft ACPI-Compliant System
(ISA) 0x000000B1 (177) Microsoft ACPI-Compliant System
(ISA) 0x000000B2 (178) Microsoft ACPI-Compliant System
(ISA) 0x000000B3 (179) Microsoft ACPI-Compliant System
(ISA) 0x000000B4 (180) Microsoft ACPI-Compliant System
(ISA) 0x000000B5 (181) Microsoft ACPI-Compliant System
(ISA) 0x000000B6 (182) Microsoft ACPI-Compliant System
(ISA) 0x000000B7 (183) Microsoft ACPI-Compliant System
(ISA) 0x000000B8 (184) Microsoft ACPI-Compliant System
(ISA) 0x000000B9 (185) Microsoft ACPI-Compliant System
(ISA) 0x000000BA (186) Microsoft ACPI-Compliant System
(ISA) 0x000000BB (187) Microsoft ACPI-Compliant System
(ISA) 0x000000BC (188) Microsoft ACPI-Compliant System
(ISA) 0x000000BD (189) Microsoft ACPI-Compliant System
(ISA) 0x000000BE (190) Microsoft ACPI-Compliant System
(PCI) 0x0000000B (11) Intel(R) 7 Series/C216 Chipset Family SMBus Host Controller - 1E22
(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E2D
(PCI) 0x00000010 (16) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 1 - 1E10
(PCI) 0x00000010 (16) Intel(R) Management Engine Interface
(PCI) 0x00000010 (16) Xeon(R) processor E3-1200 v2/3rd Gen Core processor PCI Express Root Port - 0151
(PCI) 0x00000010 (16) Xeon(R) processor E3-1200 v2/3rd Gen Core processor PCI Express Root Port - 0159
(PCI) 0x00000011 (17) Intel(R) 7 Series/C216 Chipset Family PCI Express Root Port 2 - 1E12
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family 4 port Serial ATA Storage Controller - 1E01
(PCI) 0x00000013 (19) Intel(R) 7 Series/C216 Chipset Family 2 port Serial ATA Storage Controller - 1E09
(PCI) 0x00000016 (22) High Definition Audio Controller
(PCI) 0x00000017 (23) Intel(R) 7 Series/C216 Chipset Family USB Enhanced Host Controller - 1E26
(PCI) 0xFFFFFFF8 (-8) Intel(R) 82574L Gigabit Network Connection
(PCI) 0xFFFFFFF9 (-7) Intel(R) 82574L Gigabit Network Connection
(PCI) 0xFFFFFFFA (-6) Intel(R) 82574L Gigabit Network Connection
(PCI) 0xFFFFFFFB (-5) Intel(R) 82574L Gigabit Network Connection
(PCI) 0xFFFFFFFC (-4) Intel(R) 82579LM Gigabit Network Connection
(PCI) 0xFFFFFFFD (-3) Intel(R) USB 3.0 eXtensible Host Controller
(PCI) 0xFFFFFFFE (-2) Intel(R) HD Graphics

## B.4 DMA Channel Assignments



# Appendix C

RAID & AHCI Settings

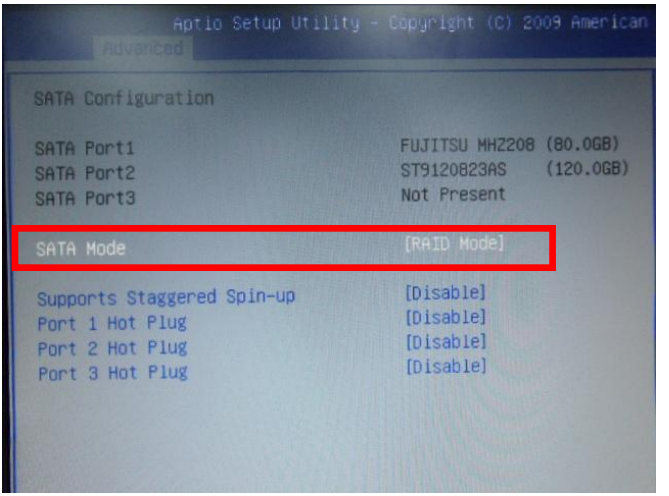
## C.1 Setting RAID

OS installation to setup RAID Mode

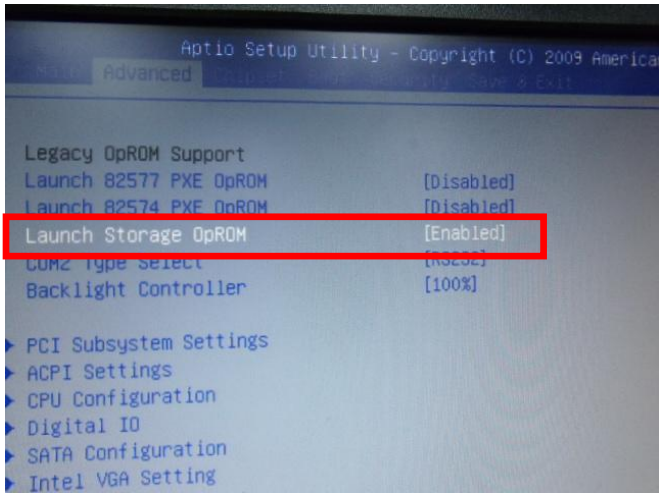
Step 1: Copy the files below from "*Driver CD ->Step 6 - RAID&AHCI"* to Disk


Step 2: Connect the USB Floppy (disk with RAID files) to the board

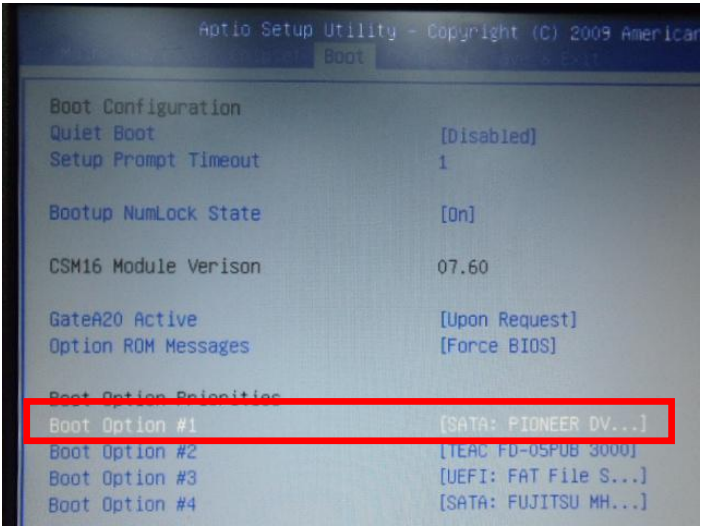
Step 3: The setting procedures " In BIOS Setup Menu"
A: Advanced -> SATA Configuration -> SATA Mode -> RAID Mode



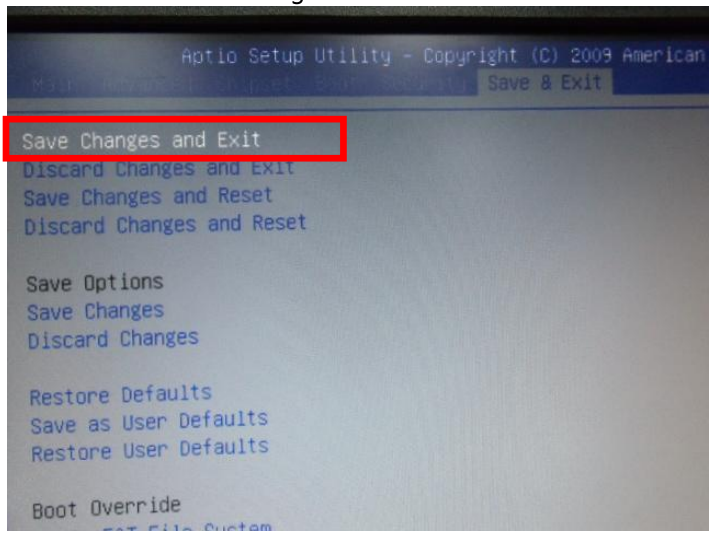

Step 4: The setting procedures "In BIOS Setup Menu"
B: Advanced -> Launch Storage OpROM -> Enabled



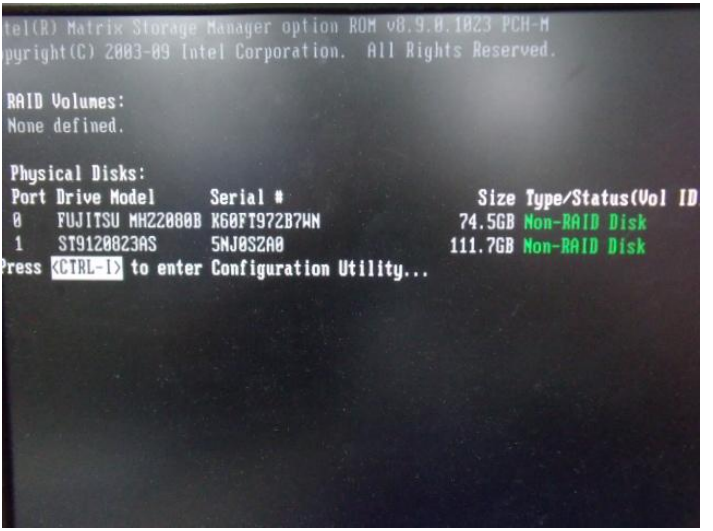
Step 5: The setting procedures "In BIOS Setup Menu"
C: Boot -> Boot Option #1 -> DVD-ROM Type



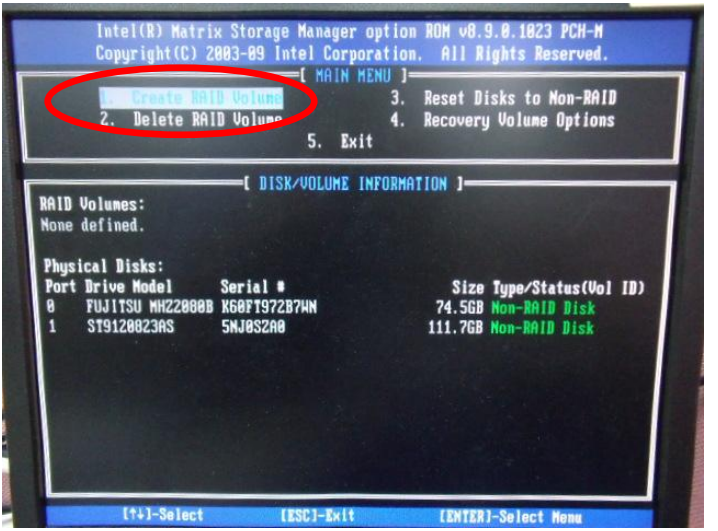

Step 6: The setting procedures "In BIOS Setup Menu"
D: Save & Exit -> Save Changes and Exit



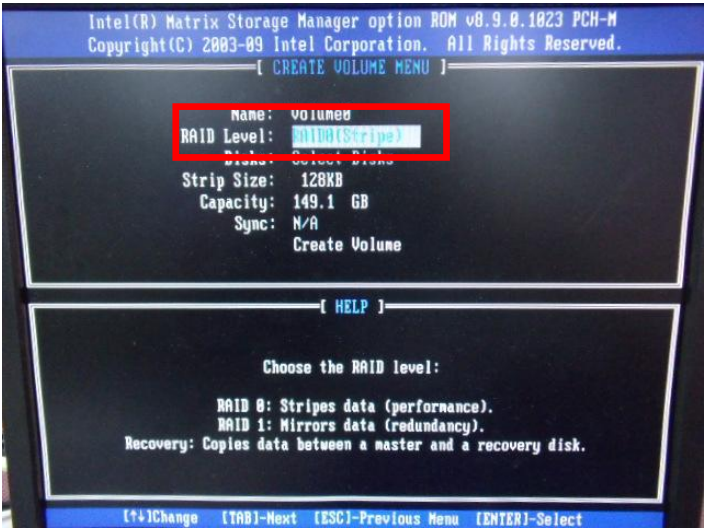
Step 7: Press Ctrl-I to enter MAIN MENU



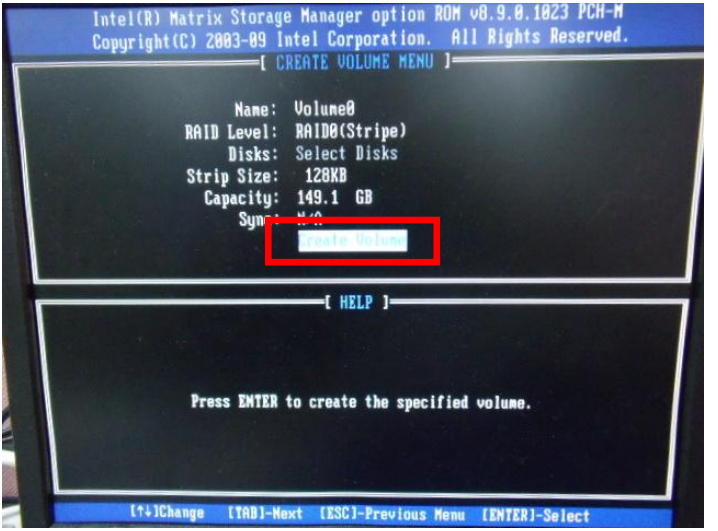

Step 8: Choose "1.Create RAID Volume"



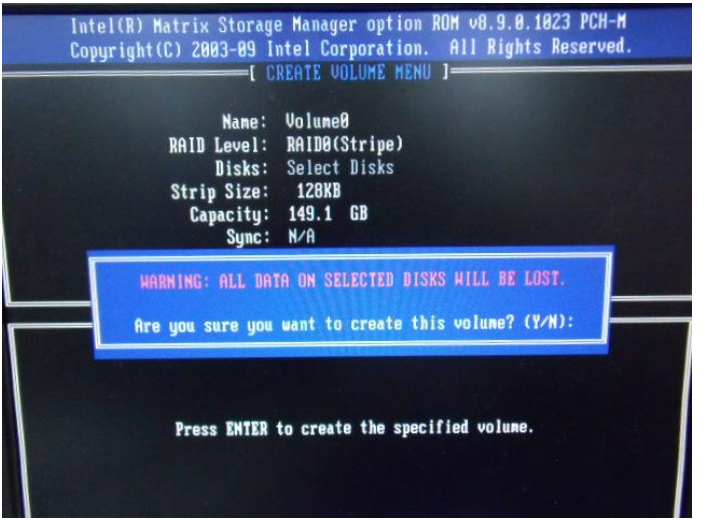
Step 9: RAID Level -> RAID0(Stripe)



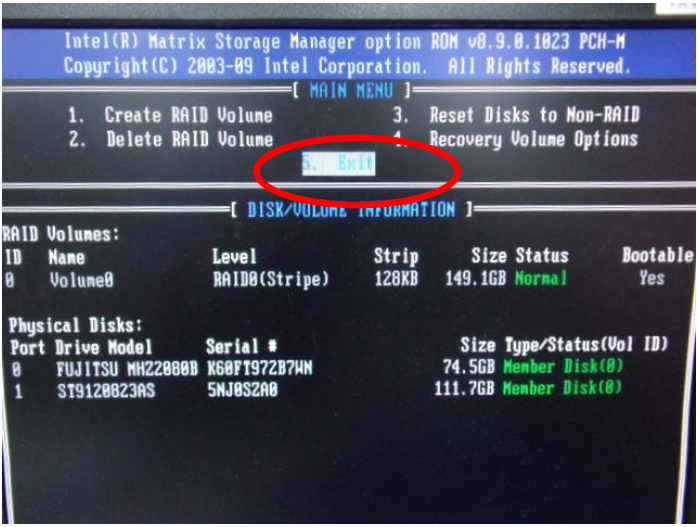

Step 10: Choose "Create Volume"



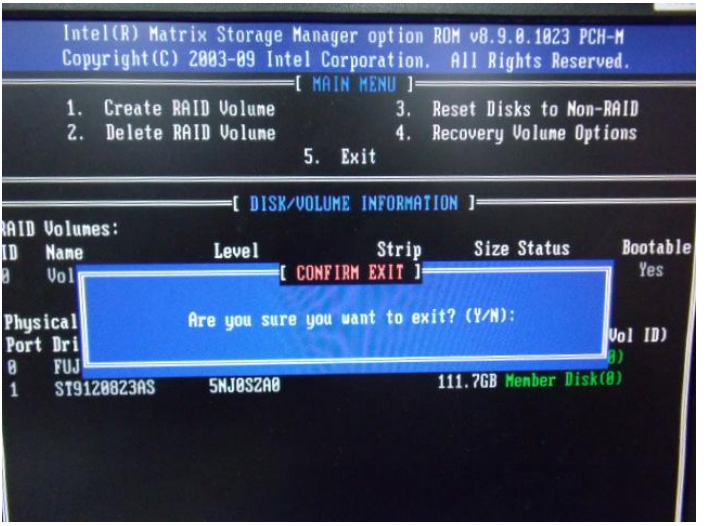
Step 11: Choose "Y"



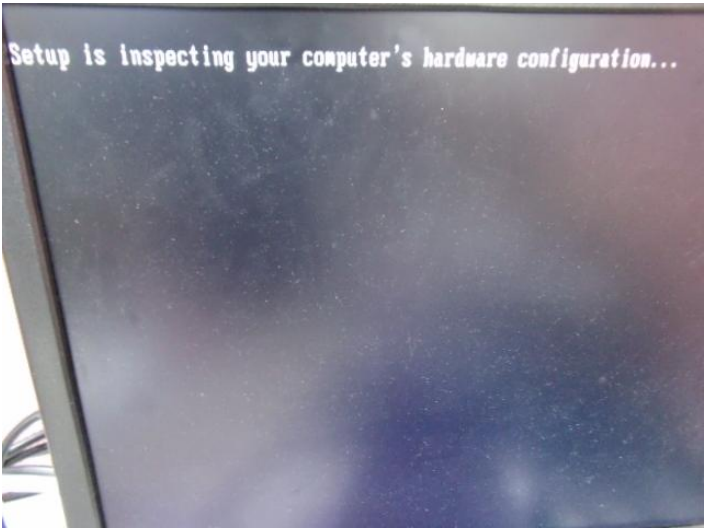

Step 12: Choose "5. Exit"



Step 13: Choose "**Y**"

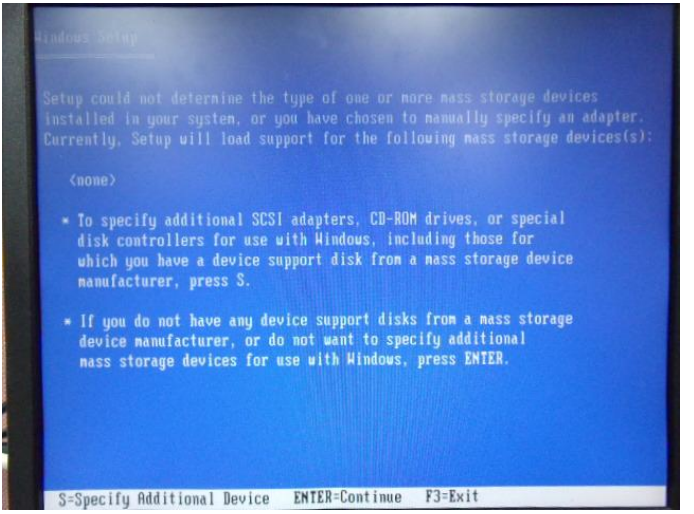



Step 14: Setup OS

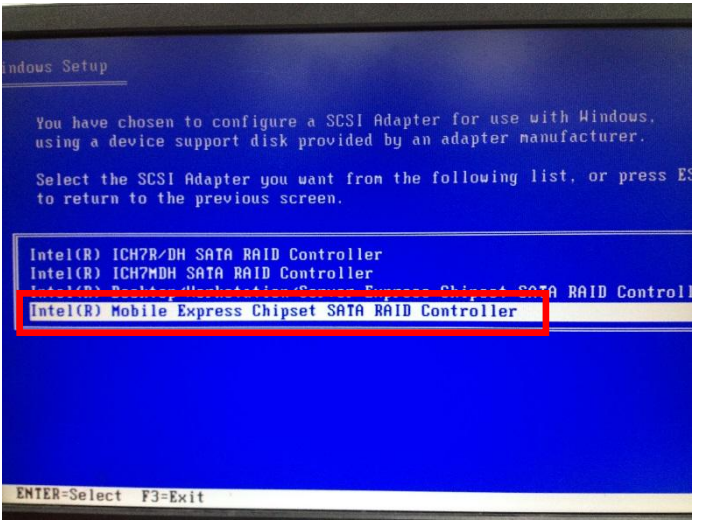


Step 15: Press "**F6**"

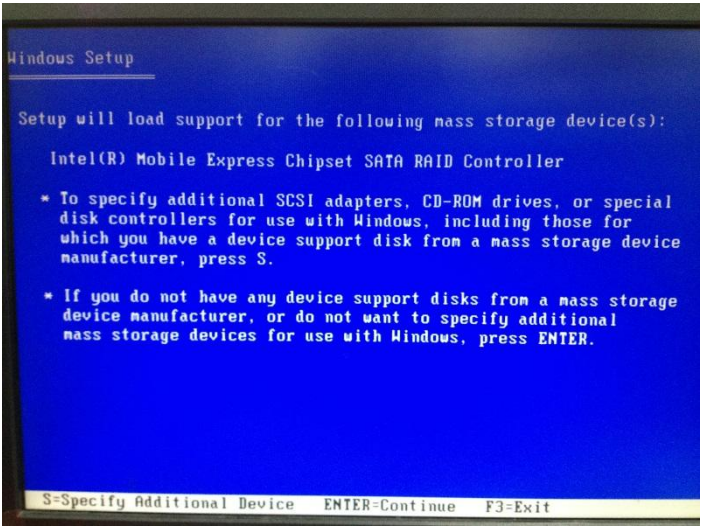

Step 16: Choose "**S**"



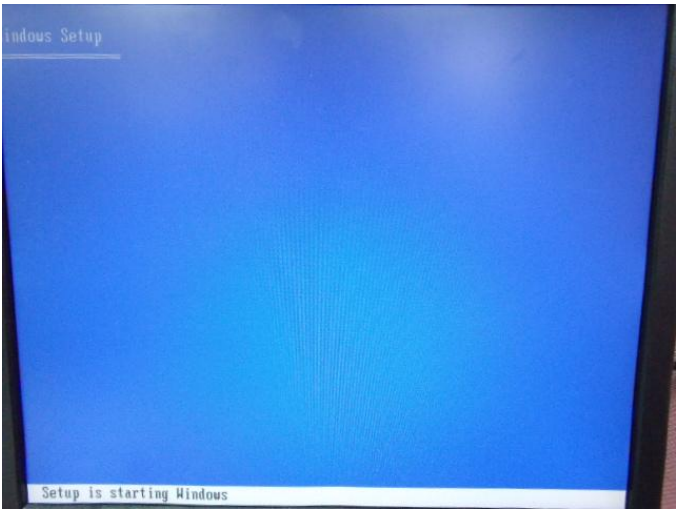
Step 17: Choose "Intel(R) Mobile Express Chipset SATA RAID Controller"




Step 18: It will show the model number you select and then press "ENTER"



Step 19: Setup is starting Windows



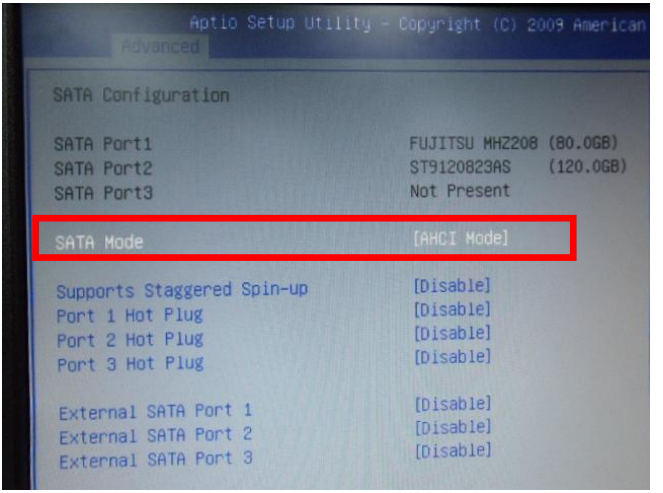
## C.2 Setting AHCI

OS installation to setup AHCI Mode

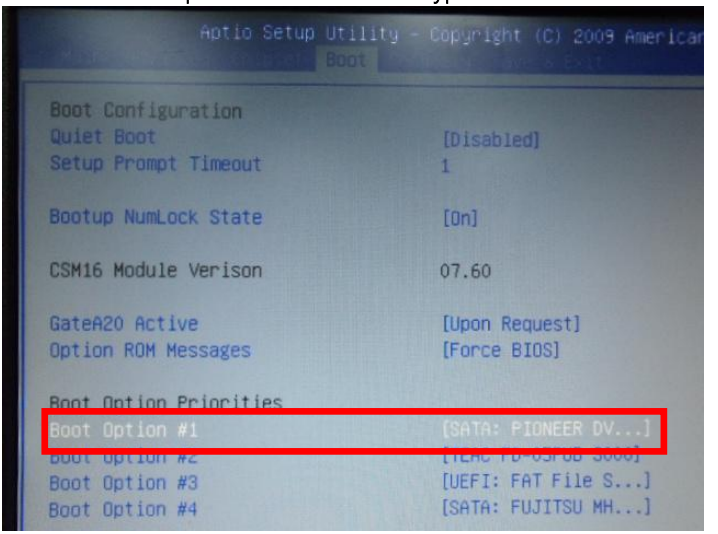
Step 1: Copy the files below from "*Driver CD ->Step 6 - RAID&AHCI"* to Disk


Step 2: Connect the USB Floppy (disk with AHCI files) to the board

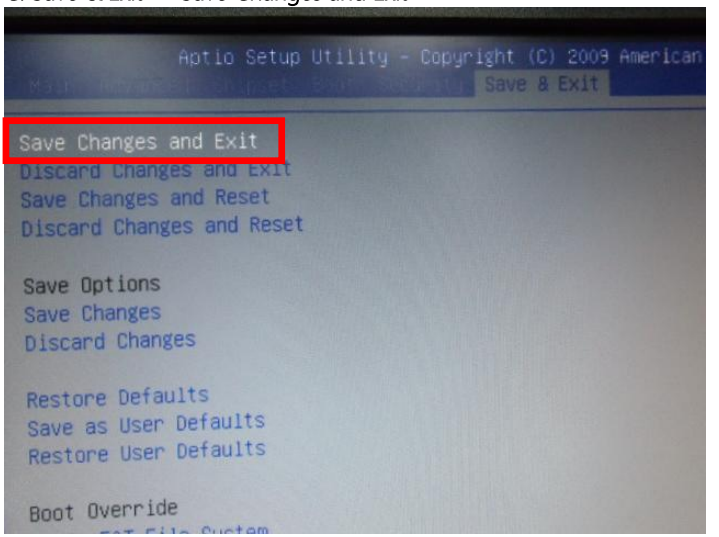
Step 3: The setting procedures " In BIOS Setup Menu"
A: Advanced -> SATA Configuration -> SATA Configuration -> SATA Mode -> AHCI Mode



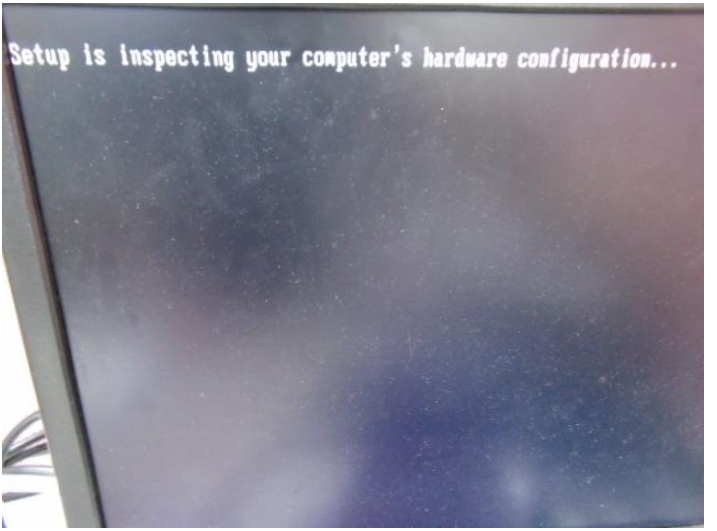

Step 4: The setting procedures "In BIOS Setup Menu"
B: Boot -> Boot Option #1 -> DVD-ROM Type



Step 5: The setting procedures "In BIOS Setup Menu"
C: Save & Exit -> Save Changes and Exit

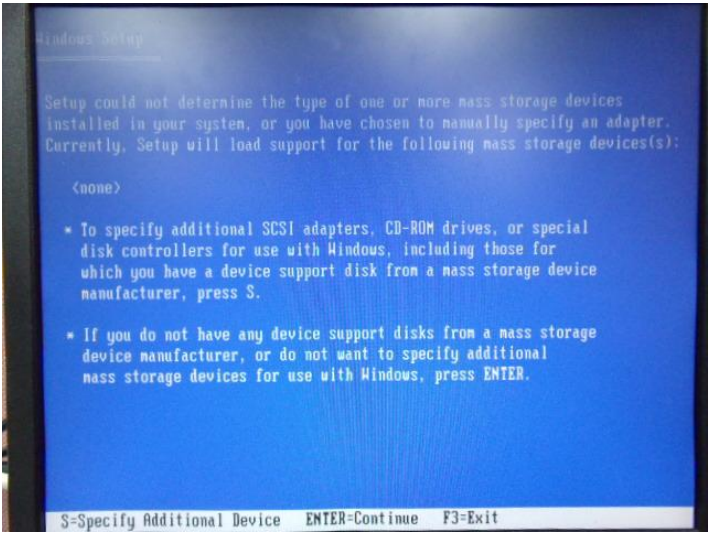



Step 6: Setup OS

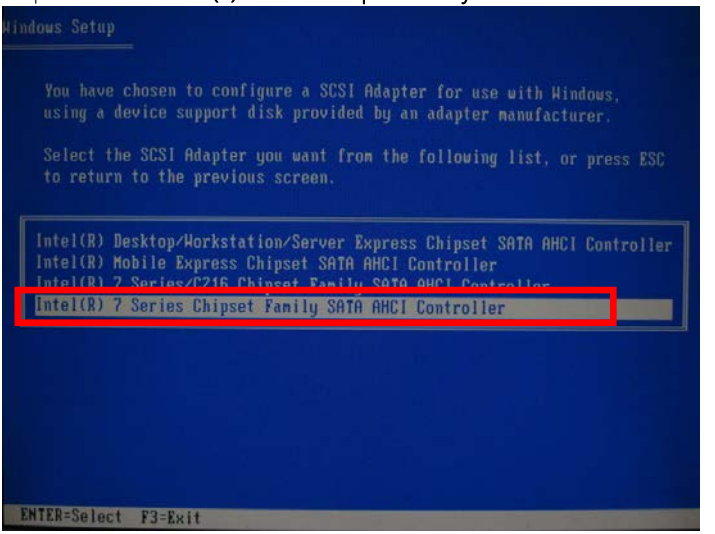


Step 7: Press "F6"

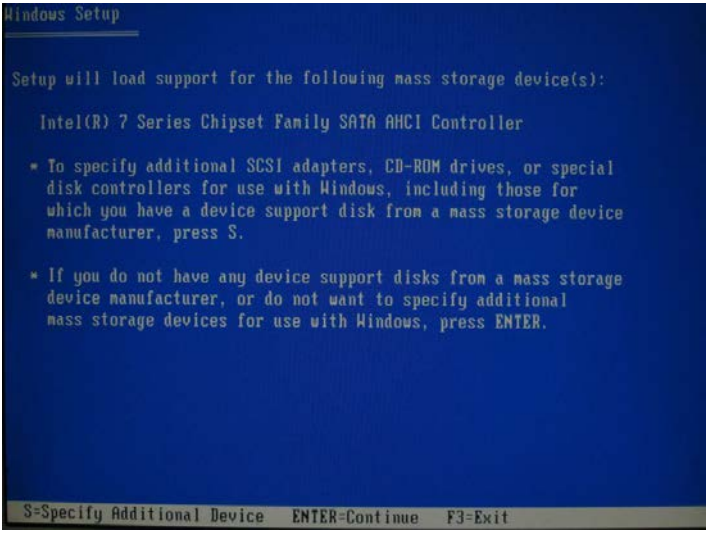

Step 8: Choose "S"



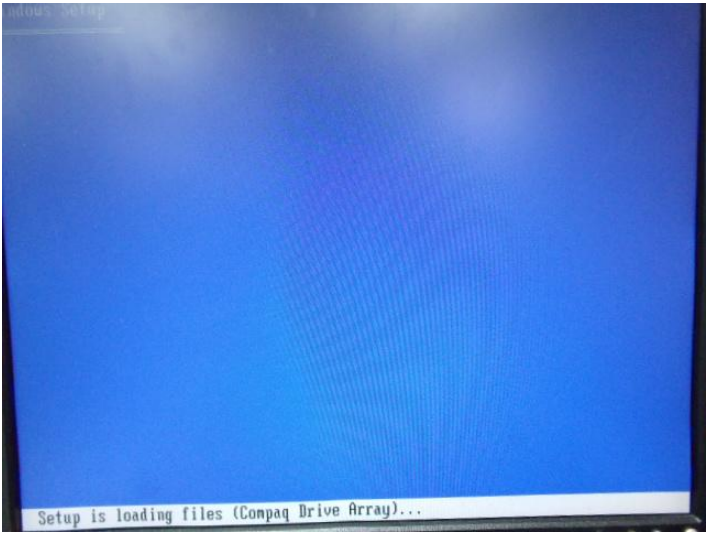
Step 9: Choose "**Intel(R) 7 Series Chipset Family SATA AHCI Controller**"




Step 10: It will show the model number you select and then press "**ENTER**"



Step 11: Setup is loading files



# Appendix D

Electrical Specifications for I/O Ports

## D.1 DIO Programming

AEC-6977 utilizes FINTEK F81866 chipset as its Digital I/O controller.

Below are the procedures to complete its configuration and the AAEON initial watchdog timer program is also attached based on which you can develop customized program to fit your application.

There are three steps to complete the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Undesired result may occur if the MB PnP Mode is not exited normally.(These three steps are the same as programming WDT)

Please be noted, the Isolation protection DIO is fixed 4 Input / 4 Output type.

DIO_P#1~4 : Input

DIO_P#5~8 : Output

## D.2 Digital I/O Register

| Table 1 : SuperIO relative register table | | |
|---|---|---|
| | Default Value | Note |
| Index | 0x2E(Note1) | SIO MB PnP Mode Index Register<br>0x2E or 0x4E |
| Data | 0x2F(Note2) | SIO MB PnP Mode Data Register<br>0x2F or 0x4F |

| Table 2 : Digital Input relative register table | | | | | |
|---|---|---|---|---|---|
| | LDN | Register | BitNum | Value | Note |
| DIO-1 Pin Status | 0x06(Note3) | 0x8A(Note4) | 0(Note5) | DI | GPIO80 |
| DIO-2 Pin Status | 0x06(Note6) | 0x8A(Note7) | 1(Note8) | DI | GPIO81 |
| DIO-3 Pin Status | 0x06(Note9) | 0x8A(Note10) | 2(Note11) | DI | GPIO82 |
| DIO-4 Pin Status | 0x06(Note12) | 0x8A(Note13) | 3(Note14) | DI | GPIO83 |
| DIO-5 Pin Status | 0x06(Note15) | 0x8A(Note16) | 4(Note17) | DO | GPIO84 |
| DIO-6 Pin Status | 0x06(Note18) | 0x8A(Note19) | 5(Note20) | DO | GPIO85 |
| DIO-7 Pin Status | 0x06(Note21) | 0x8A(Note22) | 6(Note23) | DO | GPIO86 |
| DIO-8 Pin Status | 0x06(Note24) | 0x8A(Note25) | 7(Note26) | DO | GPIO87 |

| Table 3 : Digital Output relative register table | | | | | |
|---|---|---|---|---|---|
| | LDN | Register | BitNum | Value | Note |
| DIO-1 Output Data | 0x06(Note27) | 0x89(Note28) | 0(Note29) | (Note30) | GPIO80 |
| DIO-2 Output Data | 0x06(Note31) | 0x89(Note32) | 1(Note33) | (Note34) | GPIO81 |
| DIO-3 Output Data | 0x06(Note35) | 0x89(Note36) | 2(Note37) | (Note38) | GPIO82 |
| DIO-4 Output Data | 0x06(Note39) | 0x89(Note40) | 3(Note41) | (Note42) | GPIO83 |
| DIO-5 Output Data | 0x06(Note43) | 0x89(Note44) | 4(Note45) | (Note46) | GPIO84 |
| DIO-6 Output Data | 0x06(Note47) | 0x89(Note48) | 5(Note49) | (Note50) | GPIO85 |
| DIO-7 Output Data | 0x06(Note51) | 0x89(Note52) | 6(Note53) | (Note54) | GPIO86 |
| DIO-8 Output Data | 0x06(Note55) | 0x89(Note56) | 7(Note57) | (Note58) | GPIO87 |

## D.3 Digital I/O Sample Program

```
**********************************************************************************
// SuperIO relative definition (Please reference to Table 1)
#define byte   SIOIndex   //This parameter is represented from Note1
#define byte   SIOData    //This parameter is represented from Note2
#define   void   IOWriteByte(byte IOPort, byte Value);
#define   byte   IOReadByte(byte IOPort);
// Digital Input Status relative definition (Please reference to Table 2)
#define byte   DInput1LDN    // This parameter is represented from Note3
#define byte   DInput1Reg    // This parameter is represented from Note4
#define byte   DInput1Bit    // This parameter is represented from Note5
#define byte   DInput2LDN    // This parameter is represented from Note6
#define byte   DInput2Reg    // This parameter is represented from Note7
#define byte   DInput2Bit    // This parameter is represented from Note8
#define byte   DInput3LDN    // This parameter is represented from Note9
#define byte   DInput3Reg    // This parameter is represented from Note10
#define byte   DInput3Bit    // This parameter is represented from Note11
#define byte   DInput4LDN    // This parameter is represented from Note12
#define byte   DInput4Reg    // This parameter is represented from Note13
#define byte   DInput4Bit    // This parameter is represented from Note14
#define byte   DInput5LDN    // This parameter is represented from Note15
#define byte   DInput5Reg    // This parameter is represented from Note16
#define byte   DInput5Bit    // This parameter is represented from Note17
#define byte   DInput6LDN    // This parameter is represented from Note18
#define byte   DInput6Reg    // This parameter is represented from Note19
#define byte   DInput6Bit    // This parameter is represented from Note20
#define byte   DInput7LDN    // This parameter is represented from Note21
#define byte   DInput7Reg    // This parameter is represented from Note22
#define byte   DInput7Bit    // This parameter is represented from Note23
#define byte   DInput8LDN    // This parameter is represented from Note24
#define byte   DInput8Reg    // This parameter is represented from Note25
#define byte   DInput8Bit    // This parameter is represented from Note26
**********************************************************************************
```

```
*********************************************************************************
// Digital Output control relative definition (Please reference to Table 3)
#define byte   DOutput1LDN   // This parameter is represented from Note27
#define byte   DOutput1Reg   // This parameter is represented from Note28
#define byte   DOutput1Bit   // This parameter is represented from Note29
#define byte   DOutput1Val   // This parameter is represented from Note30
#define byte   DOutput2LDN   // This parameter is represented from Note31
#define byte   DOutput2Reg   // This parameter is represented from Note32
#define byte   DOutput2Bit   // This parameter is represented from Note33
#define byte   DOutput2Val   // This parameter is represented from Note34
#define byte   DOutput3LDN   // This parameter is represented from Note35
#define byte   DOutput3Reg   // This parameter is represented from Note36
#define byte   DOutput3Bit   // This parameter is represented from Note37
#define byte   DOutput3Val   // This parameter is represented from Note38
#define byte   DOutput4LDN   // This parameter is represented from Note39
#define byte   DOutput4Reg   // This parameter is represented from Note40
#define byte   DOutput4Bit   // This parameter is represented from Note41
#define byte   DOutput4Val   // This parameter is represented from Note42
#define byte   DOutput5LDN   // This parameter is represented from Note43
#define byte   DOutput5Reg   // This parameter is represented from Note44
#define byte   DOutput5Bit   // This parameter is represented from Note45
#define byte   DOutput5Val   // This parameter is represented from Note46
#define byte   DOutput6LDN   // This parameter is represented from Note47
#define byte   DOutput6Reg   // This parameter is represented from Note48
#define byte   DOutput6Bit   // This parameter is represented from Note49
#define byte   DOutput6Val   // This parameter is represented from Note50
#define byte   DOutput7LDN   // This parameter is represented from Note51
#define byte   DOutput7Reg   // This parameter is represented from Note52
#define byte   DOutput7Bit   // This parameter is represented from Note53
#define byte   DOutput7Val   // This parameter is represented from Note54
#define byte   DOutput8LDN   // This parameter is represented from Note55
#define byte   DOutput8Reg   // This parameter is represented from Note56
#define byte   DOutput8Bit   // This parameter is represented from Note57
#define byte   DOutput8Val   // This parameter is represented from Note58
*********************************************************************************
```

```
*****************************************************************************************
VOID   Main(){
        Boolean PinStatus ;

        // Procedure : AaeonReadPinStatus
        // Input :
        //       Example, Read Digital I/O Pin 3 status
         // Output :
         //       InputStatus :
         //                0: Digital I/O Pin level is low
         //                1: Digital I/O Pin level is High
        PinStatus = AaeonReadPinStatus(DInput3LDN, DInput3Reg, DInput3Bit);

        // Procedure : AaeonSetOutputLevel
        // Input :
        //       Example, Set Digital I/O Pin 6 level
        AaeonSetOutputLevel(DOutput6LDN, DOutput6Reg, DOutput6Bit, DOutput6Val);
}
*****************************************************************************************
```

```
*****************************************************************************
Boolean    AaeonReadPinStatus(byte LDN, byte Register, byte BitNum){
        Boolean PinStatus ;

        PinStatus = SIOBitRead(LDN, Register, BitNum);
        Return PinStatus ;
}
VOID    AaeonSetOutputLevel(byte LDN, byte Register, byte BitNum, byte Value){
        ConfigToOutputMode(LDN, Register, BitNum);
        SIOBitSet(LDN, Register, BitNum, Value);
}
*****************************************************************************
```

```
*******************************************************************************
VOID   SIOEnterMBPnPMode(){
       IOWriteByte(SIOIndex, 0x87);
       IOWriteByte(SIOIndex, 0x87);
}

VOID   SIOExitMBPnPMode(){
       IOWriteByte(SIOIndex, 0xAA);
}

VOID   SIOSelectLDN(byte LDN){
        IOWriteByte(SIOIndex, 0x07); // SIO LDN Register Offset = 0x07
       IOWriteByte(SIOData, LDN);
}

VOID   SIOBitSet(byte LDN, byte Register, byte BitNum, byte Value){
       Byte TmpValue;

       SIOEnterMBPnPMode();
        SIOSelectLDN(byte LDN);
       IOWriteByte(SIOIndex, Register);
       TmpValue = IOReadByte(SIOData);
       TmpValue &= ~(1 << BitNum);
       TmpValue |= (Value << BitNum);
       IOWriteByte(SIOData, TmpValue);
       SIOExitMBPnPMode();
}

VOID   SIOByteSet(byte LDN, byte Register, byte Value){
       SIOEnterMBPnPMode();
        SIOSelectLDN(LDN);
       IOWriteByte(SIOIndex, Register);
        IOWriteByte(SIOData, Value);
        SIOExitMBPnPMode();
}
*******************************************************************************
```

```
*****************************************************************************************
Boolean    SIOBitRead(byte LDN, byte Register, byte BitNum){
        Byte TmpValue;

        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, Register);
         TmpValue = IOReadByte(SIOData);
        TmpValue &= (1 << BitNum);
        SIOExitMBPnPMode();
        If(TmpValue == 0)
                Return 0;
        Return 1;
}
VOID   ConfigToOutputMode(byte LDN, byte Register, byte BitNum){
        Byte TmpValue, OutputEnableReg;

        OutputEnableReg = Register-1;
        SIOEnterMBPnPMode();
         SIOSelectLDN(LDN);
         IOWriteByte(SIOIndex, OutputEnableReg);
         TmpValue = IOReadByte(SIOData);
         TmpValue |= (1 << BitNum);
         IOWriteByte(SIOData, OutputEnableReg);
         SIOExitMBPnPMode();
}
*****************************************************************************************
```