AAEON Technology INC.
ISO-9001/ISO-14001 Certified
Industrial Automation PCs

Design Guide for Q7 Carrier Board

Version 1.0

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Chapter 1 Introduction

1.1. Scope of the Application Note of Carrier Board

This document is a design guide for implementing a system carrier board for Q7 CPU modules. And, it is especially for AAEON Q7 CPU modules, such as AQ7-LN, AQ7-BT, AQ7-iMX6, etc. This guide includes reference design for the mechanical design, heat spreader implementation, as well as external circuitry

required to implement the miscellaneous peripheral functions. This guide also shows how to extend the related peripheral devices or expansion slots on Q7 module. The reader is assumed to have the knowledge like USB, SATA, PCI Express, LVDS and PC related peripheral interface.
This document provides information about design reference information of the carrier board for the Q7 modules from AAEON Technology Inc. No warranty of suitability, purpose or fitness is implied. All of the design and content in this document is subject to be changed without notice.

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1.2. Glance of the Carrier Board and Legend

Q7 Module utilizes one 230-pin high-density connector to interface the Q7 CPU module and carrier board. This connector may provide the signals: (depend on vary Q7 modules)
- Up to 8 USB ports
- Up to 2 SATA ports
- Up to 4 PCI Express x1 connectors
- 1 LVDS: Dual LVDS channels support 18/24/36/48 bits LCD
- SDVO port
- Audio AC97 interface
- Single Ethernet interface for 10/100/1000 Ethernet
- LPC Bus
- Power management signals
- +5V primary power supply input
- +5V standby and +3.3V RTC power supply input

PS: Analog VGA: It has to use a 10-pin cable to connect Q7 CPU module and carrier board.

1.3. Block Diagram of Carrier Board for Q7

Figure 1-1 shows the ECB-970 block diagram

Figure 1-1 ECB-970 Block Diagram

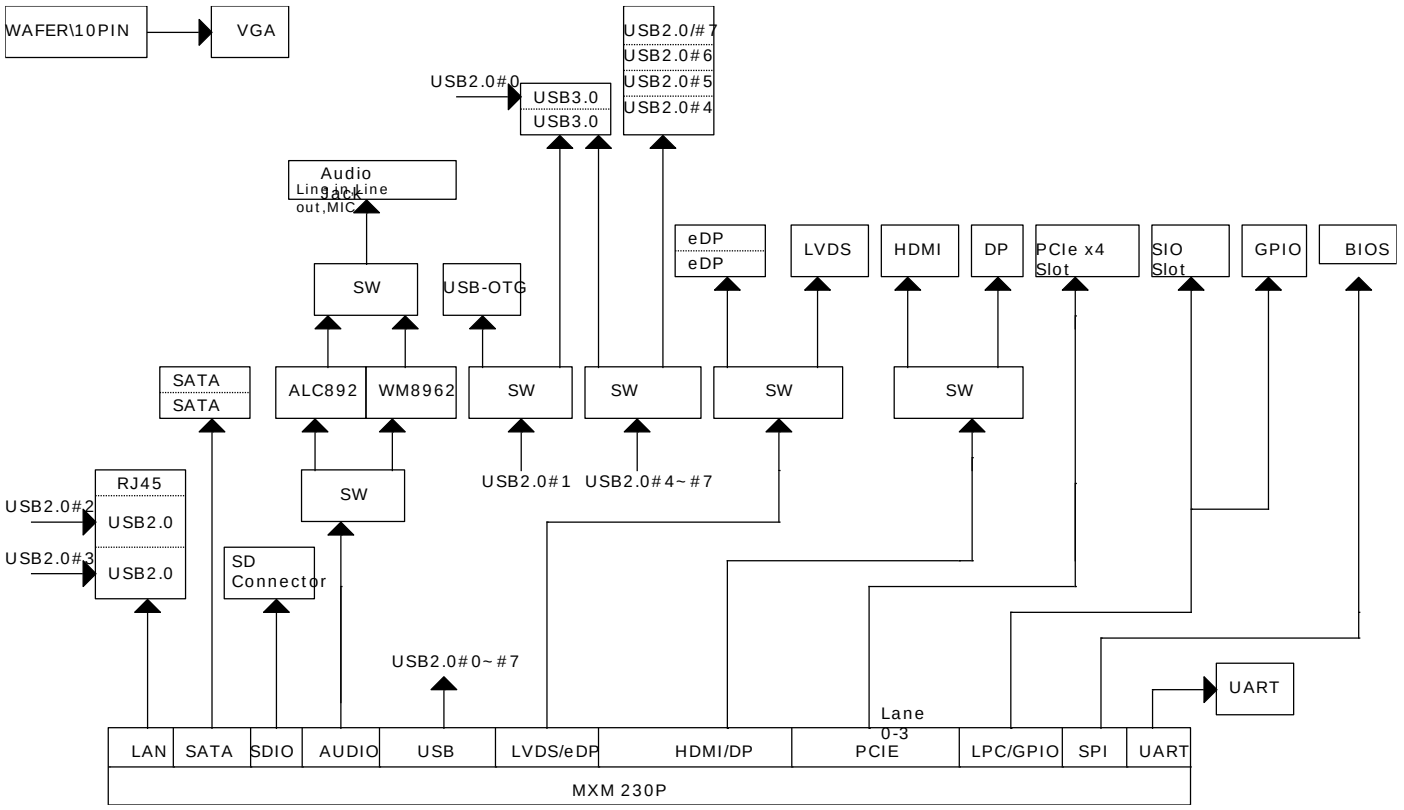


Figure 1-2 ECB-970 Power Diagram

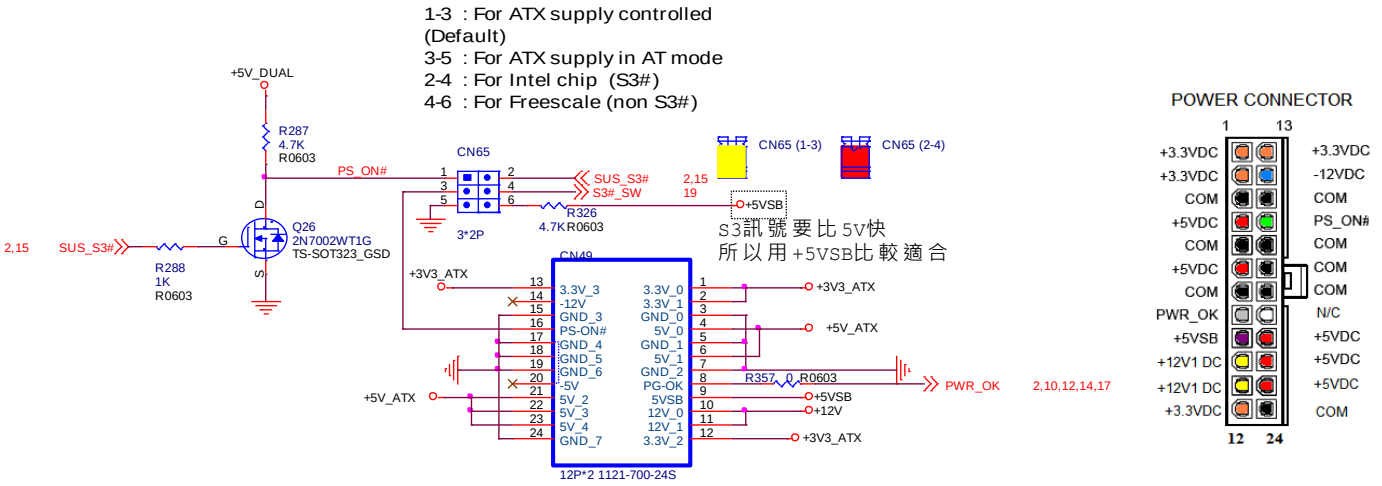


Figure 1-2 shows the ECB-970 power design.

1.4. Legend and Notice for Schematic Drawing

Figure 1-3 Legend of the symbols to be used in following schematic

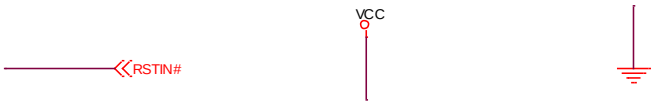


Figure 1-3 (a) **Figure 1-3** (b) **Figure 1-3** (c)

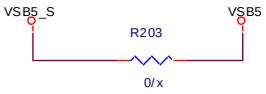


Figure 1-3 (d)

In order for reader to read the schematic easily, **Figure 1-3** illustrates several popular symbols, which will be used in schematic example of this application note. **Figure 1-3** (a) shows RSTIN# will be connected to another worksheet. **Figure 1-3** (b) and (c) are for VCC power and ground of the circuit respectively. **Figure 1-3** (d) shows VSB5_S connects with VSB5 through R203. **Figure 1-3 (d) R203 value 0/X means 0 ohm but not populate.**

In the following section of Chapter 2, the components had been annotated in the schematic.
- 5VSB: It is from 5VSB (Standby +5V from ATX power supply).
- VCC5: It's +5V from ATX or AT power supply when power is turned on.

In the following schematic, we have omitted most of the decoupling/bypass capacitors to simplify this application note. Consequently, reader must add those components when designs the carrier board.

1.5. ATX Power Sequence

1.5.1 ATX Power Sequence for +12 VDC and +5 VDC , +3.3 VDC

The +12 VDC and +5 VDC output levels must be equal to or greater than the +3.3 VDC output at all times during power-up and normal operation. The time between the +12 VDC or +5 VDC output reaching its minimum in-regulation level and +3.3 VDC reaching its minimum in-regulation level must be ≤ 20 ms.

(Refer : ATX12V Power Supply Design Guide_ Version 2.2)

Figure 1-4 ATX Power Supply Timing

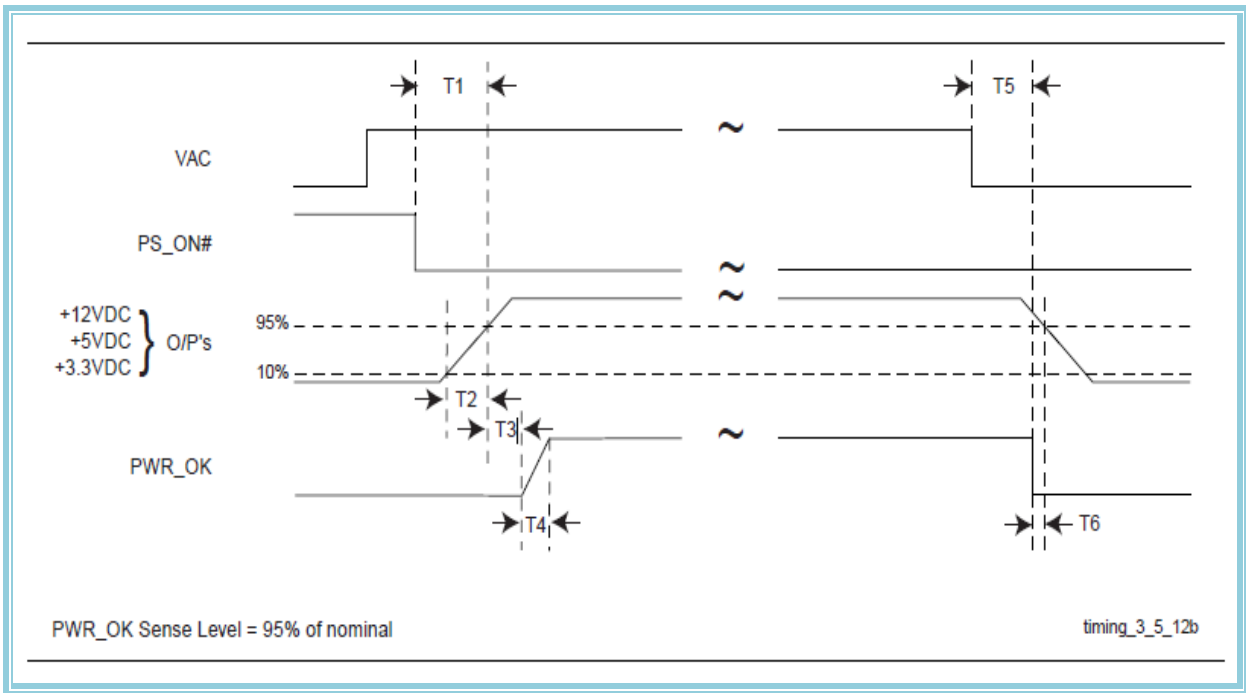


Table 1-5: ATX Power Signals Timing

Signal Type	Timing
Power-on Time	T1 < 500 ms
Rise time	0.1 ms ≤ T2 ≤ 20 ms
PWR_OK delay	100 ms < T3 < 500 ms
PWR_OK rise time	T4 ≤ 10 ms
AC loss to PWR_OK hold-up time	T5 ≥ 16 ms
Power-down warning	T6 ≥ 1 ms

1.5.2 ATX vs AT Supplies

ATX power supplies are in common use in contemporary PCs. ATX supplies have two sets of power rails: a set for normal operation (12V, 5V, 3.3V and -12V) and a separate 5V Suspend rail. The 5V Suspend rail is present whenever the ATX supply has AC input power. The other rails are on only when a control signal from the PC hardware known as PS_ON# is held low by the motherboard, allowing software control of the power supply. The PC motherboard may implement several mechanisms for controlling the AC power, including a push button switch that switches a low voltage logic signal rather than the AC main power.

Other options may be implemented, including the capability to turn on the main power on events such as a keyboard press, mouse activity, etc.
AT power supplies do not have a Suspend rail and do not allow software control of the power supply. An AT supply is on when the supply is connected to the AC main and the power switch that is in series with the AC main input is on. AT supplies are extinct in the commercial PC market, but the term lives on as a reference to a power supply that does not allow software control.

An ATX supply may be converted to AT style operation by simply holding the ATX PS_ON# input low all the time.

1.5.3 ATX and AT Power state

Table 1-6: Power state

State	Description	Comment
G3	Mechanical Off	System power consumption is near zero – the only power consumption is that of the RTC circuits, which are powered by a backup battery.
S5	Soft Off	System is off except for a small subset that is powered by the 5V Suspend rail.
S4	Suspend to Disk	System is off except for a small subset that is powered by the 5V Suspend rail. (that is powered off).
S3	Suspend to RAM	System is off except for system subset that includes the RAM. Suspend power is provided by the 5V Suspend rail.
S0	On	System is on.

Table 1-7: Signals SUS_S5#, SUS_S4# and SUS_S3# Power States

State	SUS_S5#	SUS_S4#	SUS_S3#
G3	NA	NA	NA
S5	Low	Low	Low
S4	High	Low	Low
S3	High	High	Low
S0	High	High	High

1.5.4 ATX and AT Power Sequence

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 64 below. A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 65 below.

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details.

Figure 1-8 ATX Sequence

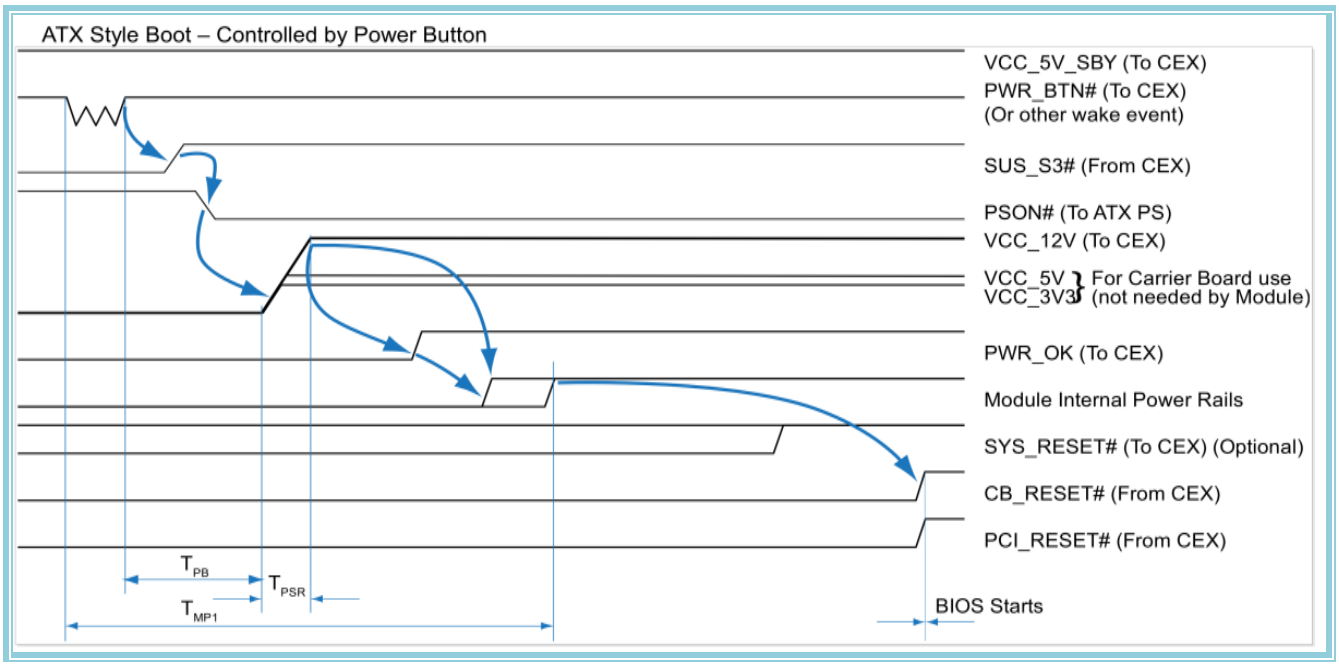


Figure 1-9 AT Sequence

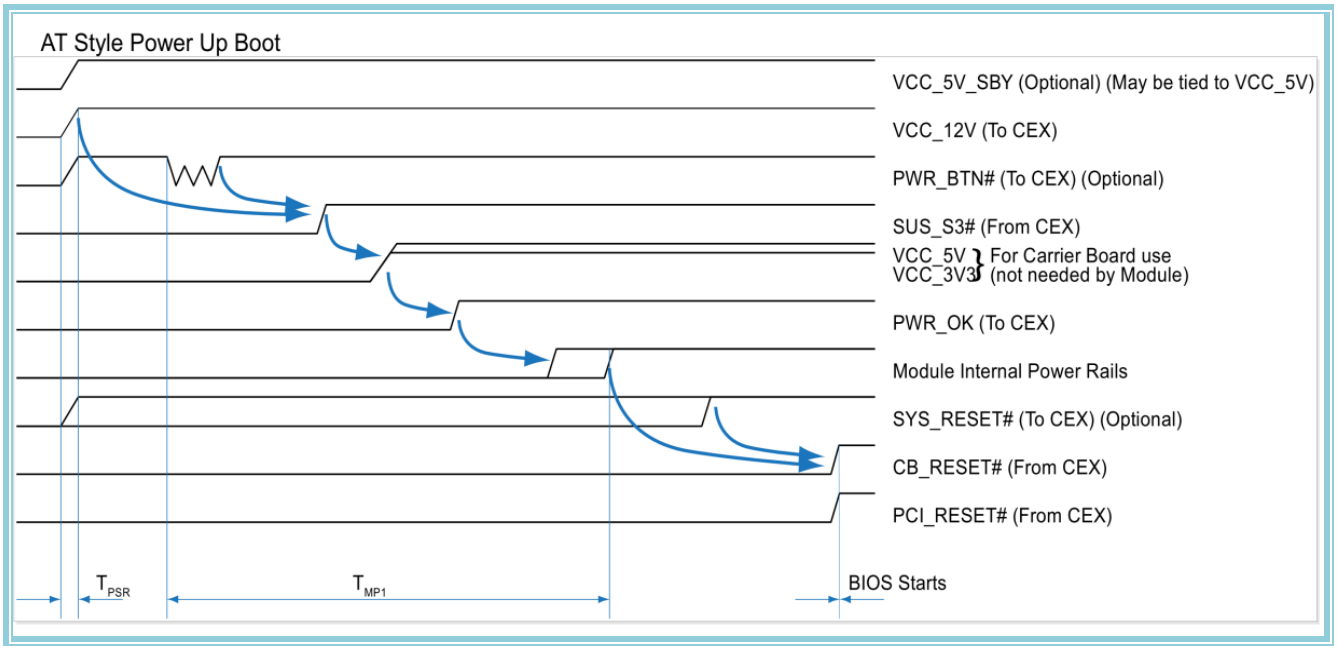


Table 1-10: ATX and AT Power Up Timing Values

Parameter	Min Value	Max Value	Description	Comments
TPB	10ms	500ms	Push Button Power Switch – time to bring Module chipset out of Suspend mode	Applies only to ATX Style Power Up
TPSR	0.1ms	20ms	Power Supply Rise Time	

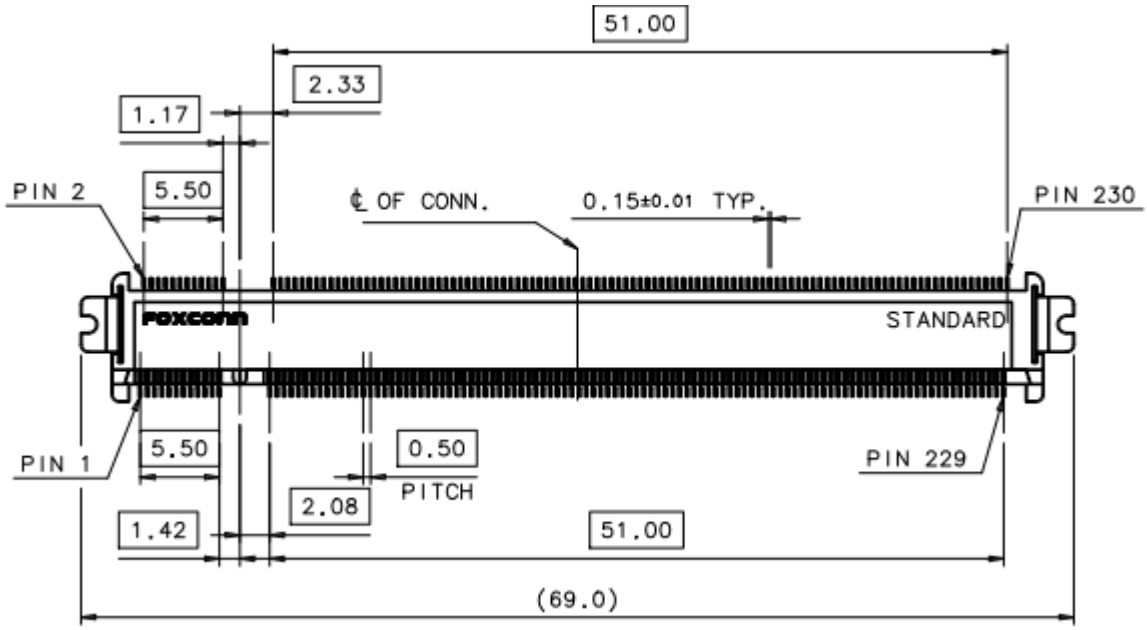
Chapter 2 Schematic and Connection

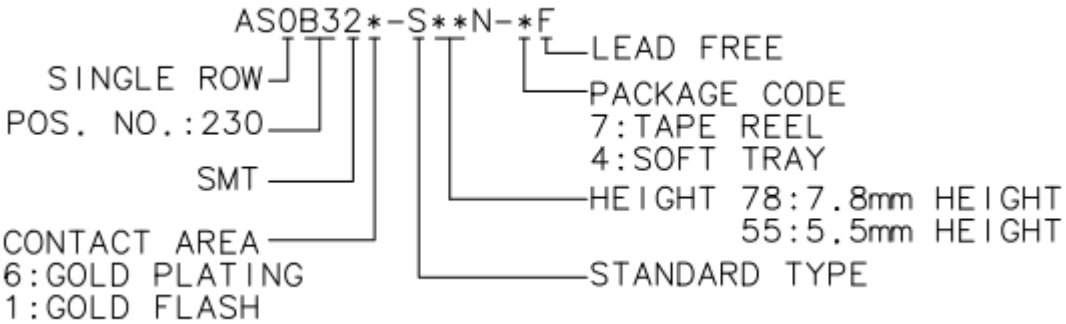
This chapter will introduce all of the interconnection circuit and related circuit to support the functionalities of this carrier board. Hence, we will have the following sections to describe the suggestion for the implementation.

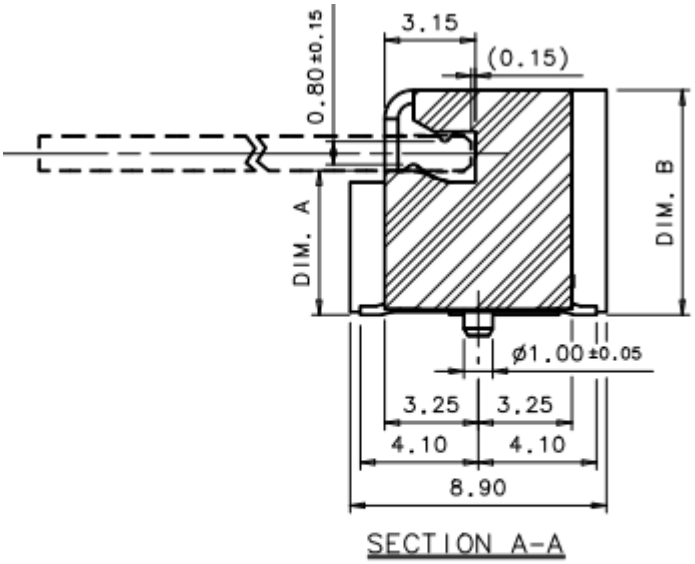
2.1. Inter–connection Connector

Connector: (TF) SOCKET CONNECTOR.230P.90D.(F).MXM 0.5mm. FOXCONN.AS0B321-S78N- 4F

Figure 2-1 Photo for MXM connector



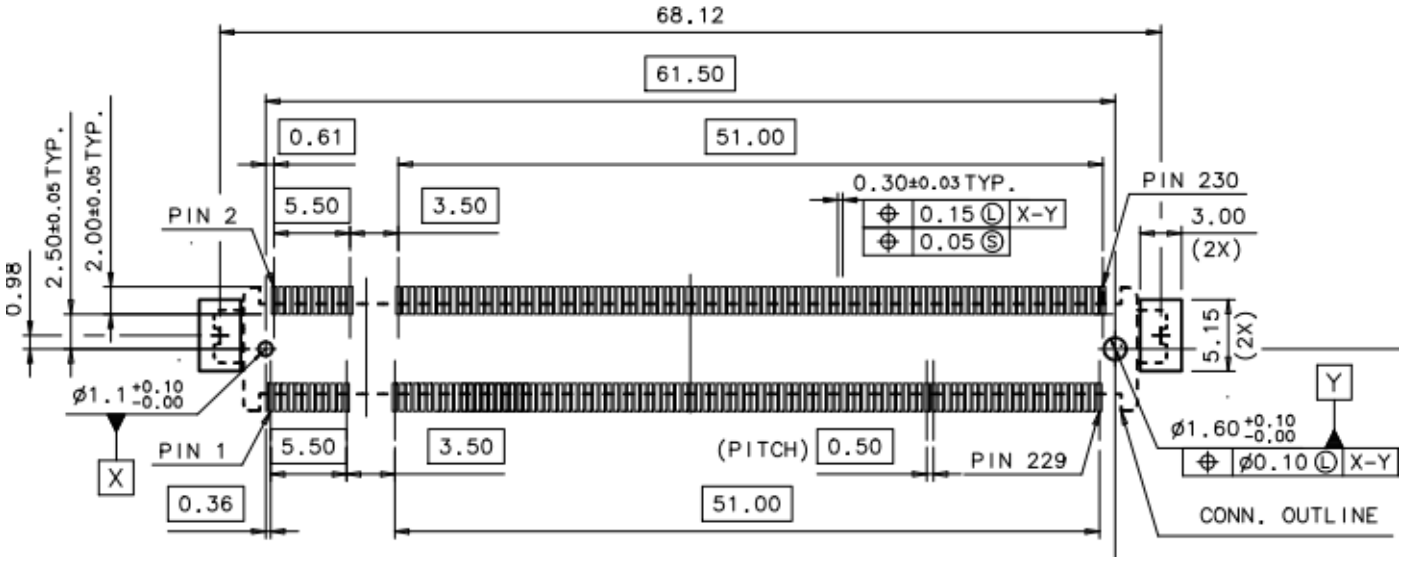




DIM. A	DIM. B
2.7	5.5
5.0	7.8

Note: Current capacity per pin: 500mA

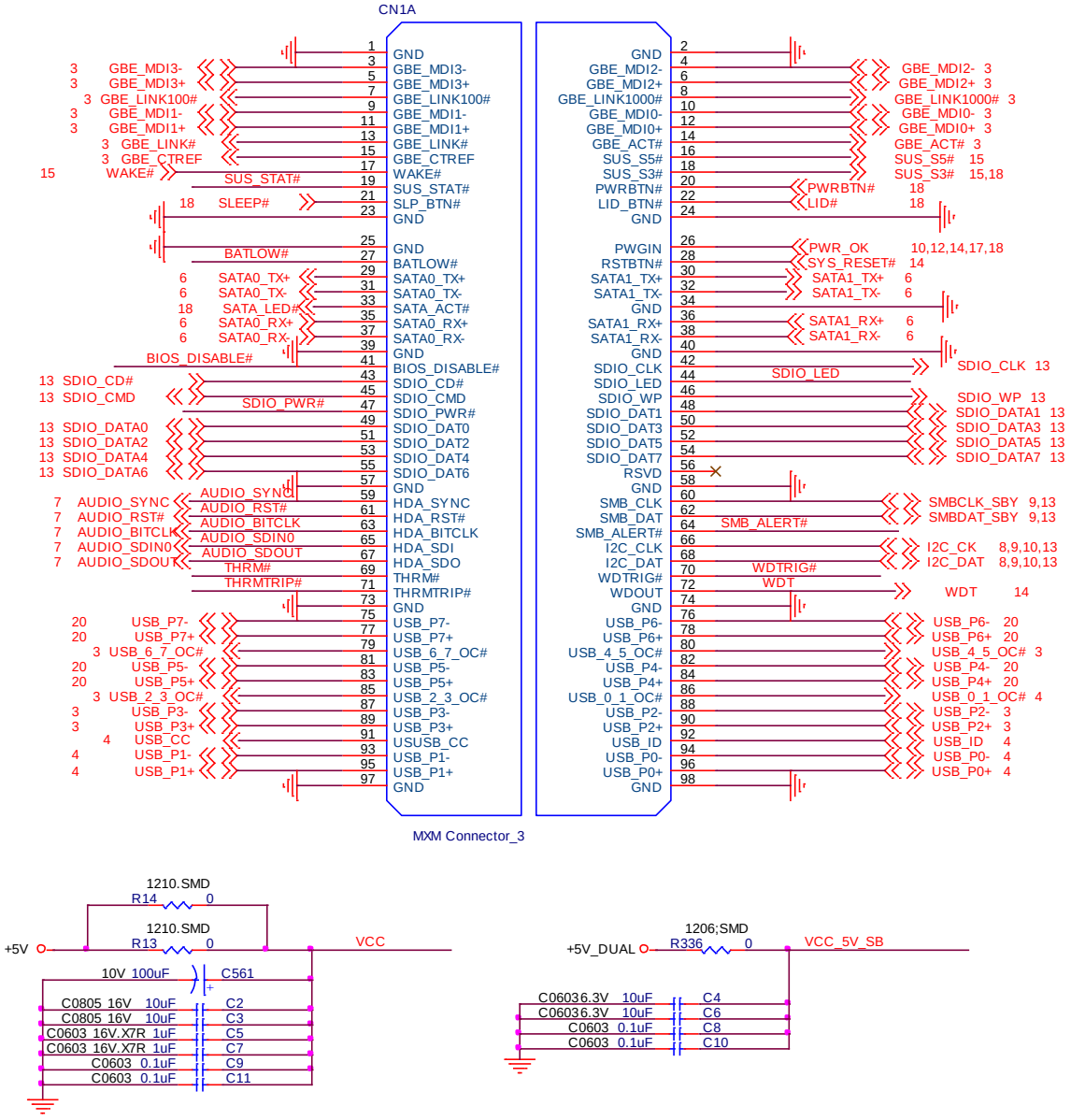
Figure 2-2 Footprint of MXM connector

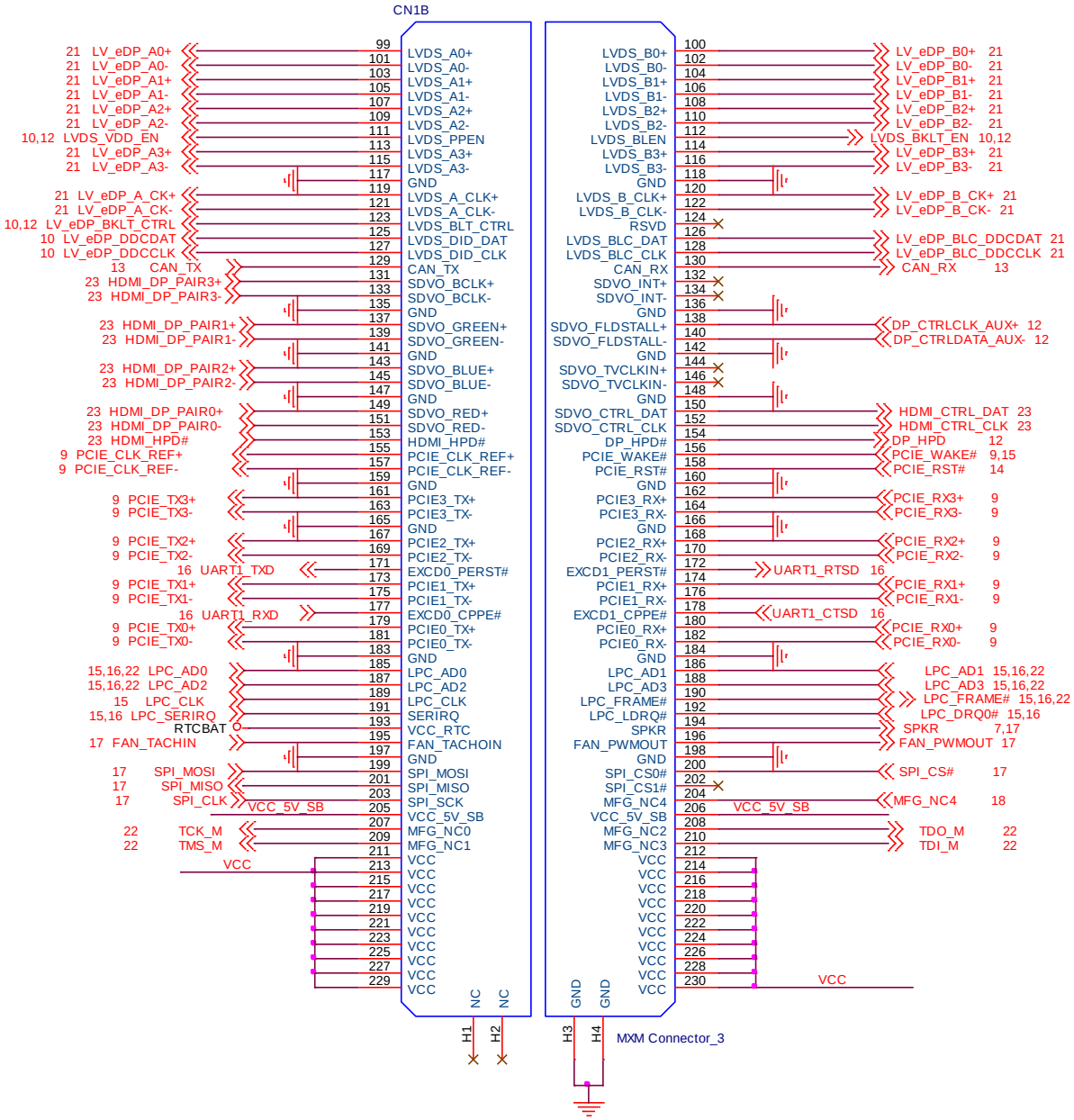


2.2. Connector CN1 and Schematic

Figure 2-3 shows CN1 connector for interfacing Q7 module to ECB-970.

Figure 2-3 CN1 schematic



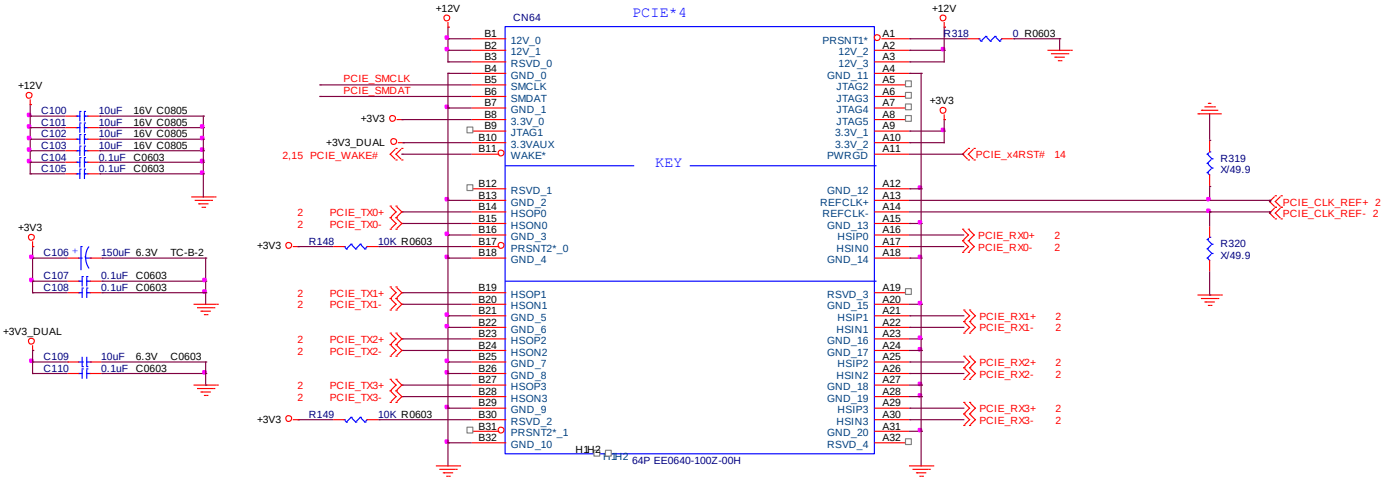

CN1B
MXM Connector_3

2.3. PCI Express Schematic

2.3.1. PCIE*4 Schematic

ECB-970 supports PCIE*4 slot. The following is its application schematic.

Figure 2-4 PCIE*4 schematic



2.3.2. PCI Express Layout guide

Table 1 PCI Express layout guide

Parameter	Definition
Differential impedance target	100Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S) (intra-pair)	6 mils (Dependent on stack)
Trace spacing (S) (inter-pair)	20 mils
Reference plane	GND referencing preferred GND stitching vias required next to signal vias
Length matching within differential pair (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict requirement Please route the RX signals and TX signals of each link to each other on the same layer.
Length matching between CLK and CLK# pairs (intra-pair)	Max. 5 mils
Length matching between PCIESLOT1_CLK and PCIECLOT2_CLK pairs (inter-pair)	No strict requirement
AC coupling capacitors	100 nF for TX lines have implemented on Q7 modules. 100 nF for RX lines have to be implemented on customer's carrier board.
VIA usage (carrier board)	Max. 2
Signal length (L) (carrier board)	Max. 7.7 inches to PCIE device Max. 14.5 inches to PCIE slot

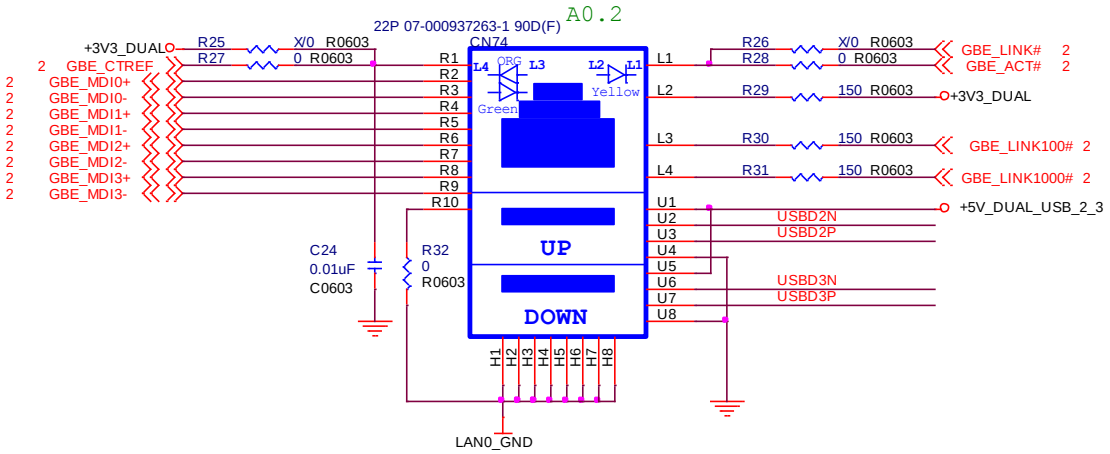
Notes: Please have PCB vendor calculate the correct PCB impedance.

2.4. Gigabit Ethernet connector Schematic

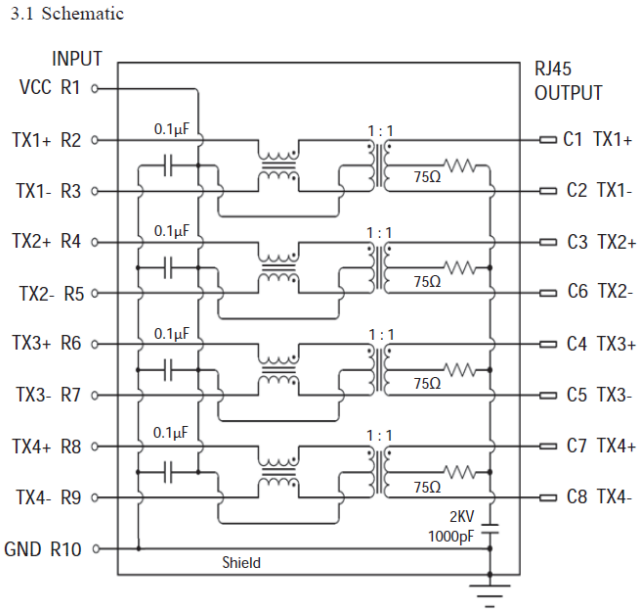
2.4.1. Gigabit ethernet schematic

Figure 2-5 Gigabit ethernet signals are from Q7 CPU module.

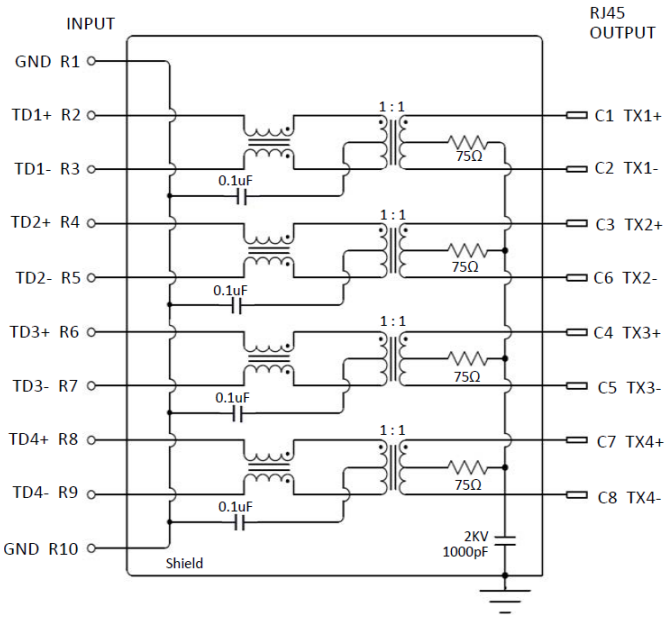
Figure 2-5 Gigabit Ethernet connector Schematic



For AQ7-LN and AQ7-BT, The connector P/N is UDE 07-000937263-1.



For AQ7-iMX6, the LAN chip vendor asked the following RJ-45 requirement. Please refer the following. The connector P/N is UDE 07-000939A33-1.



2.4.2. Gigabit ethernet layout guide

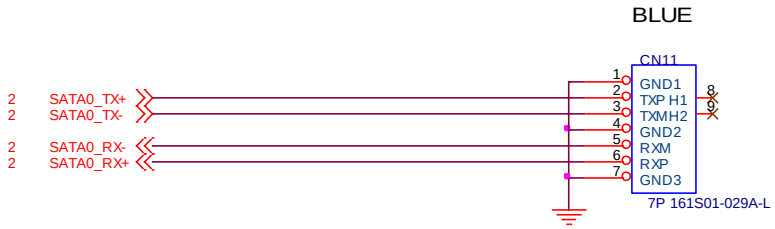
Table 2 Gigabit ethernet layout guide

Parameter	Definition
Differential impedance target	95Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S) (within the pair)	6 mils (Dependent on stack)
Trace spacing (S) (between pairs)	50 mils
Reference plane	GND referencing preferred
Length matching within differential pair	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	Max. 30 mils
VIA usage (carrier board)	Max. 2
Signal length (L) (carrier board)	4 inches In order to have better eye diagram, please keep it as short as possible

2.5. SATA connector Schematic

2.5.1. SATA Connector Schematic

Figure 2-6 SATA Connector Diagram



2.5.2. SATA layout guide

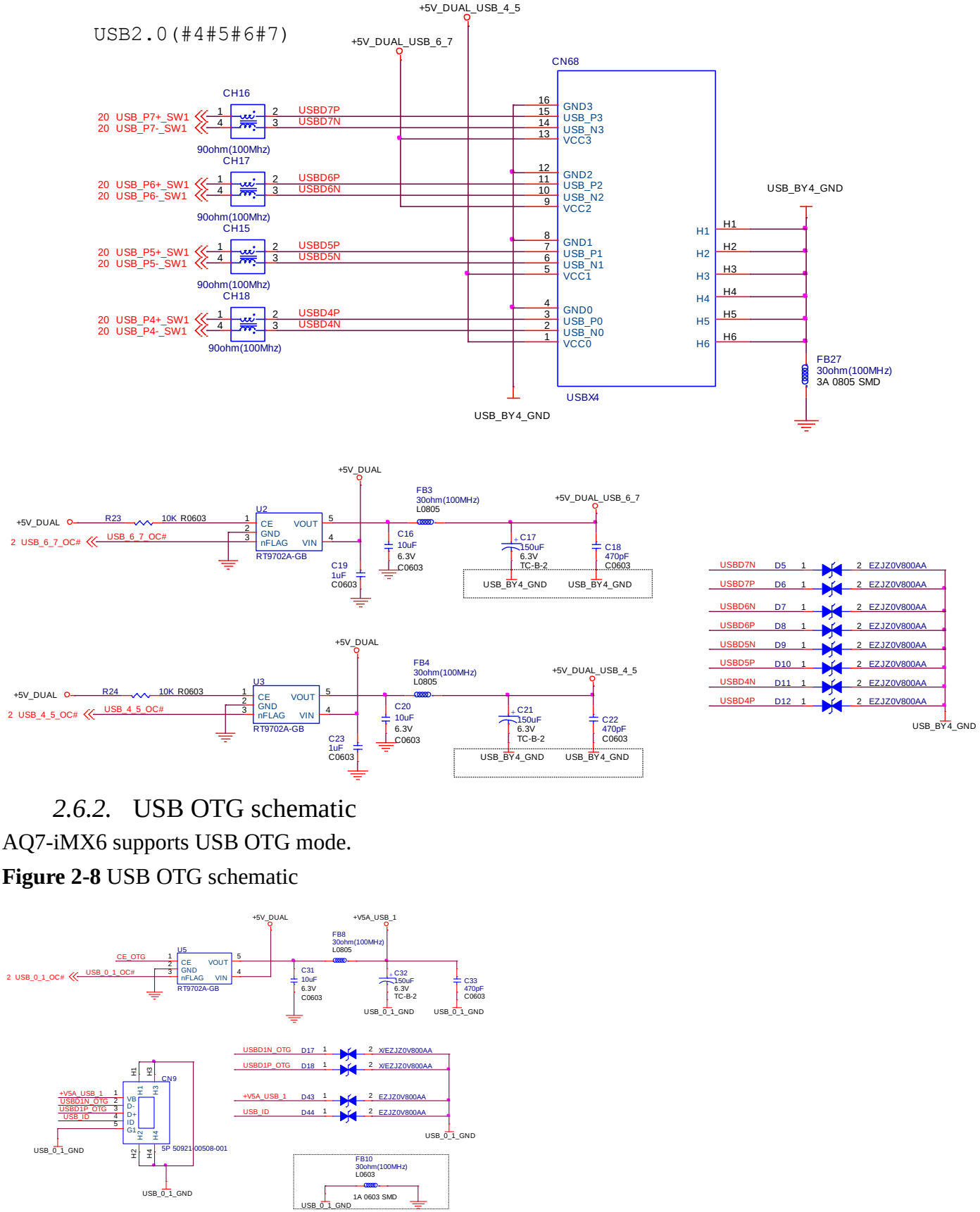
Table 3 SATA layout guide

Parameter	Definition
Differential impedance target	100Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S) (intra-pair)	6 mils (Dependent on stack)
Trace spacing (S) (inter-pair)	20 mils
Reference plane	GND referencing preferred GND stitching vias required next to signal vias
Length matching within differential pair (intra-pair)	Max. 5 mils
Length matching between RX and TX pairs (inter-pair)	No strict requirement Please route the RX signals and TX signals of each link to each other on the same layer.
AC coupling capacitors	AC Caps for TX and RX lines have implemented on Q7 modules.
Signal length (L)	Max. 2.5 inches Please keep it as short as possible

2.6. USB Connection

2.6.1. USB schematic

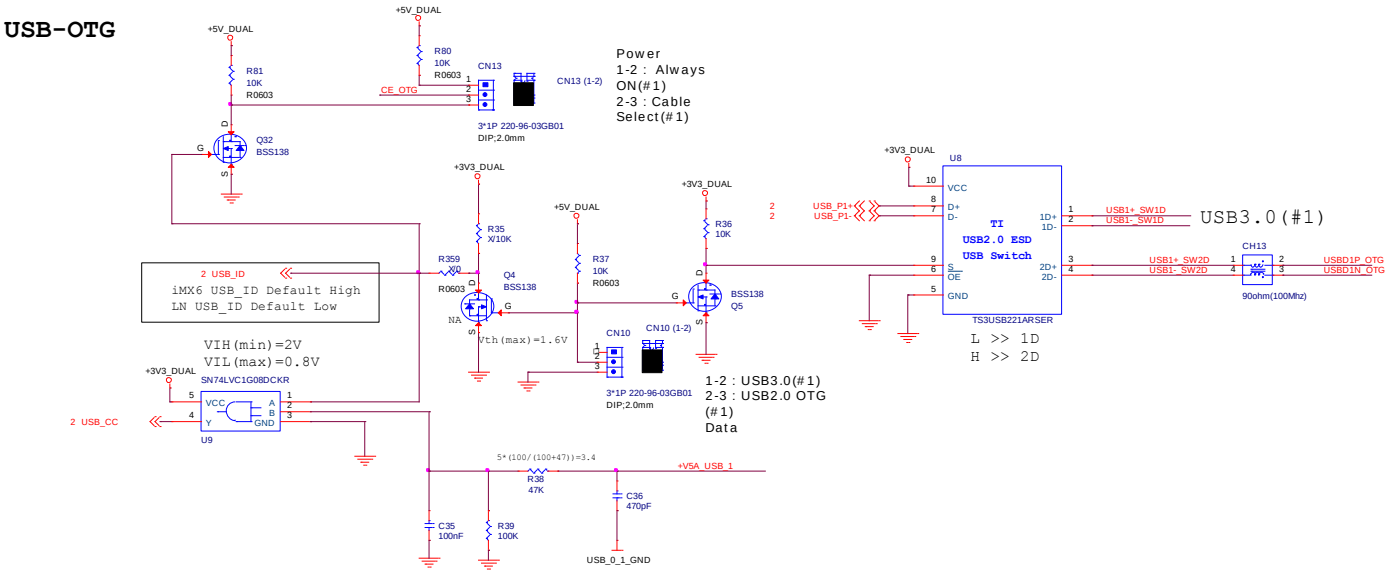
Figure 2-7 USB schematic



2.6.2. USB OTG schematic

AQ7-iMX6 supports USB OTG mode.

Figure 2-8 USB OTG schematic



2.6.3. USB layout guide

Table 4 USB layout guide

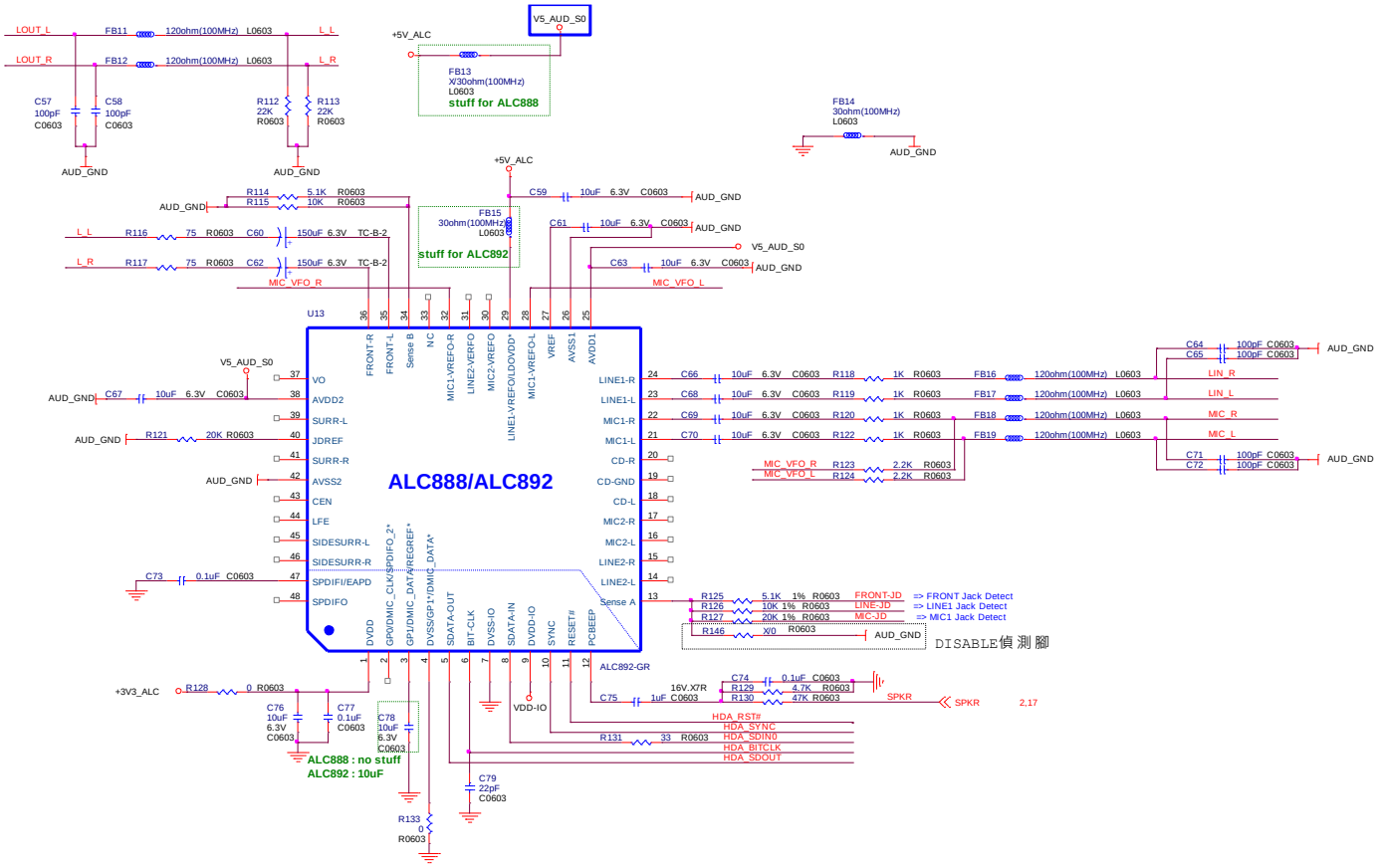
Parameter	Definition
Differential impedance target	90Ω ± 15%
Trace width (W)	5 mils (Dependent on stack)
Trace spacing (S) (intra-pair)	6 mils (Dependent on stack)
Trace spacing (S) (inter-pair)	20 mils
Reference plane	GND referencing preferred GND stitching vias required next to signal vias
Length matching within differential pair (intra-pair)	Max. 5 mils
Signal length (L) (carrier board)	Max. 14 inches

2.7. High Definition Audio Connection

2.7.1. ALC892 schematic

ALC892 is for AQ7-LN and AQ7-BT HDA CODEC.

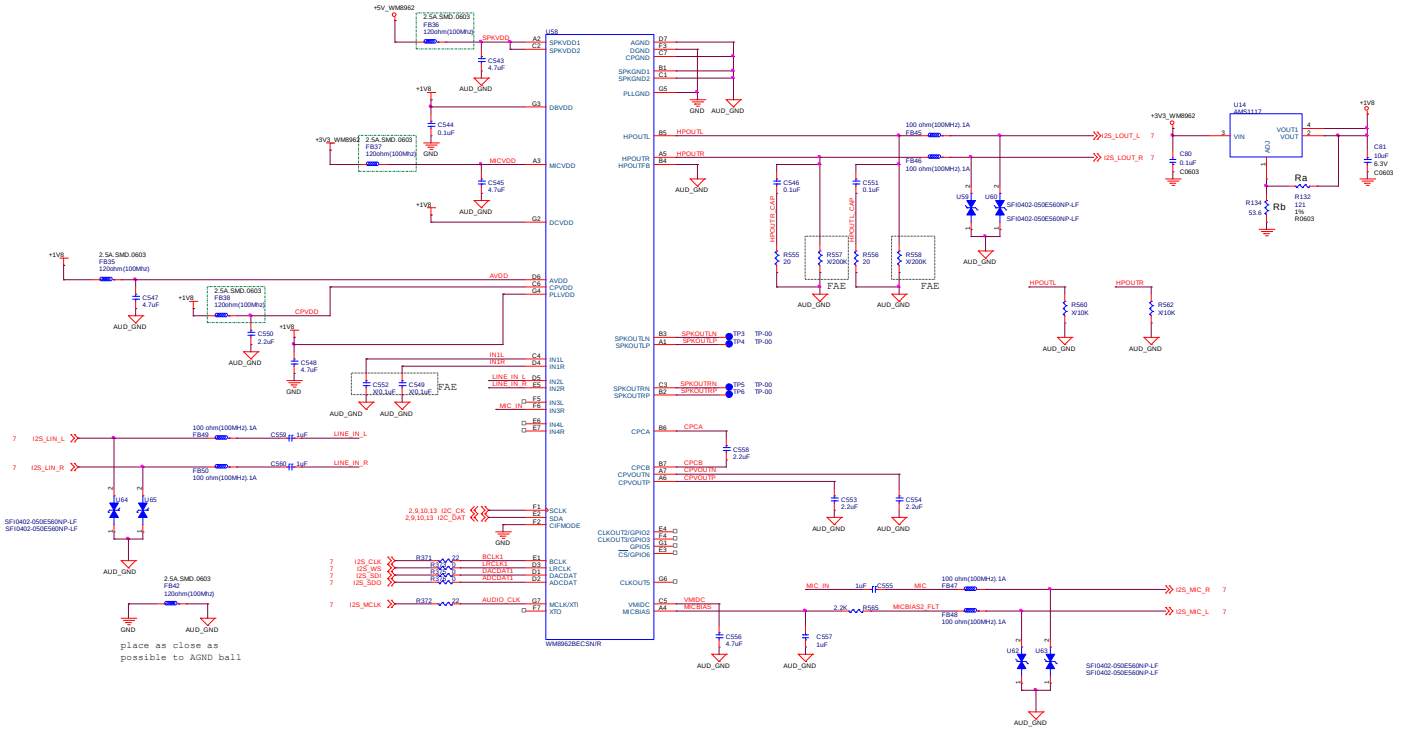
Figure 2-9 ALC892 schematic



2.7.2. I2S Audio

The following is the WM8962B schematic for AQ7-IMX6 I2S interface. The WM8962B is a low power, high performance stereo CODEC designed for portable digital audio applications. There is stereo class D speaker drivers provide 2W per channel into 4 Ohm BTL loads, with a 5V supply.

Figure 2-10 WM8962B schematic



2.7.3. Audio layout guide

Table 5 Audio layout guide

Parameter	Definition
Impedance target	55Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S)	12 mils (Dependent on stack)
Length matching within HDA_RST#, HDA_SYNC, HDA_SDIN0, HDA_BIT_CLK,HDA_SDOUT	100 mils
Signal length (L) (carrier board)	Max. 10 inches

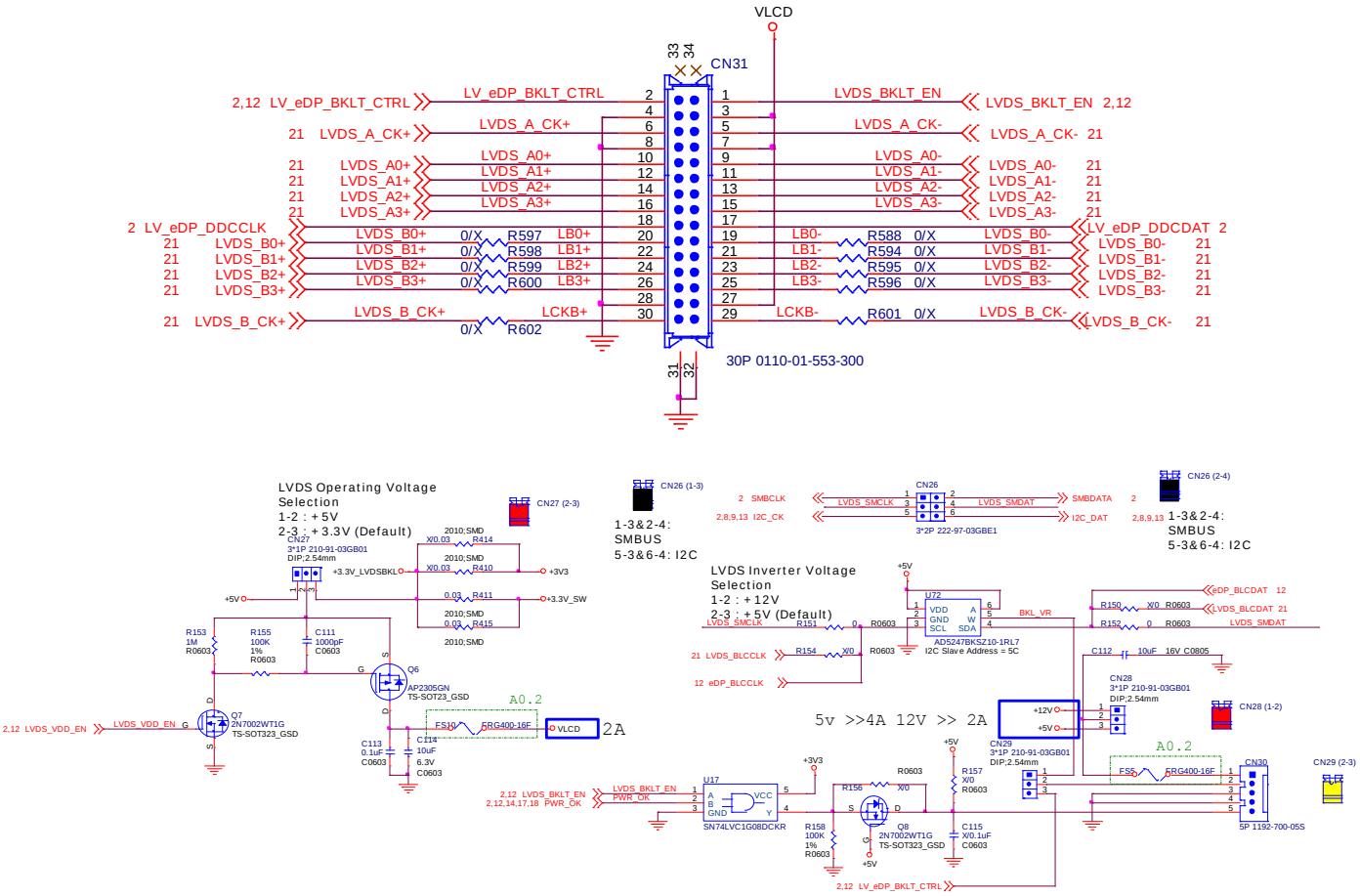
Note: 1. Partition the board with all analog components grouped together in one area and all digital components in another.

2. Locate analog and digital signals as far as possible from each other.

2.8. LVDS Connection

2.8.1. LVDS schematic

Figure 2-11 LVDS Connection



2.8.2. LVDS layout guide

Table 6 LVDS layout guide

Parameter	Definition
Differential impedance target	95Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S) (intra-pair)	6 mils (Dependent on stack)
Trace spacing (S) (inter-pair)	20 mils
Reference plane	GND referencing preferred GND stitching vias required next to signal vias
Length matching within differential pair (intra-pair)	Max. 5 mils
Length matching between clock and data pairs	Max. 20 mils
Signal length (L) (carrier board)	Max. 3.8 inches

2.9. LPC Interface

2.9.1. LPC IO Slot

The LPC IO slot is for AQ7-LN and AQ7-BT that support the LPC Bus.

Figure 2-12 LPC IO Slot

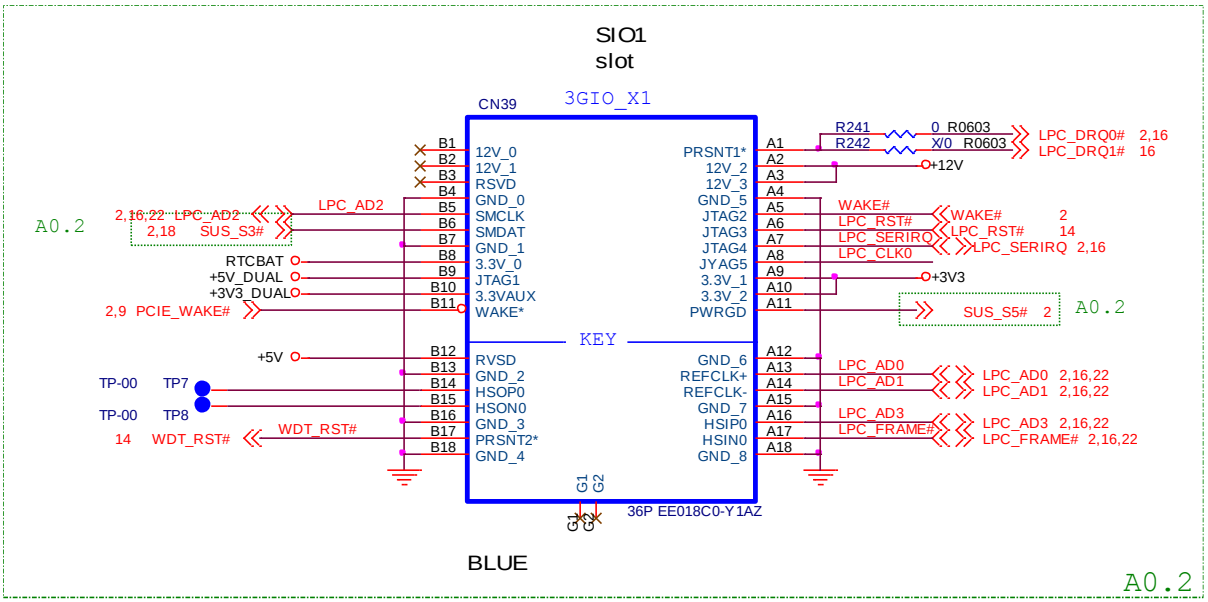
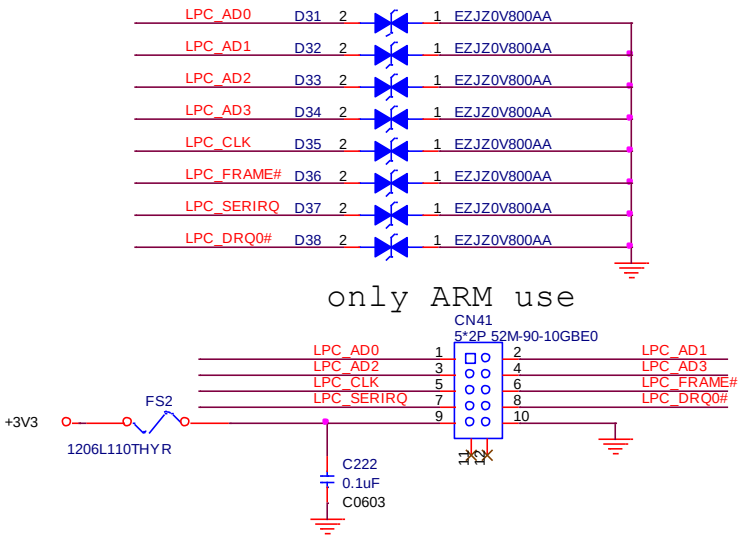


Figure 2-13 Digital I/O Schematic



2.9.1. LPC layout guide

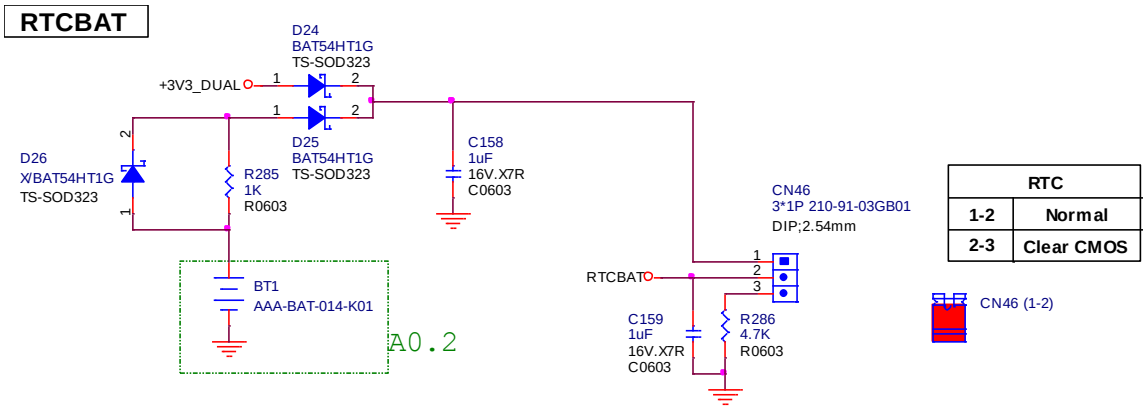
Table 7 LPC layout guide

Parameter	Definition
Impedance target	55Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S)	12 mils (Dependent on stack)

2.10. Peripheral Connection

2.10.1. Battery schematic

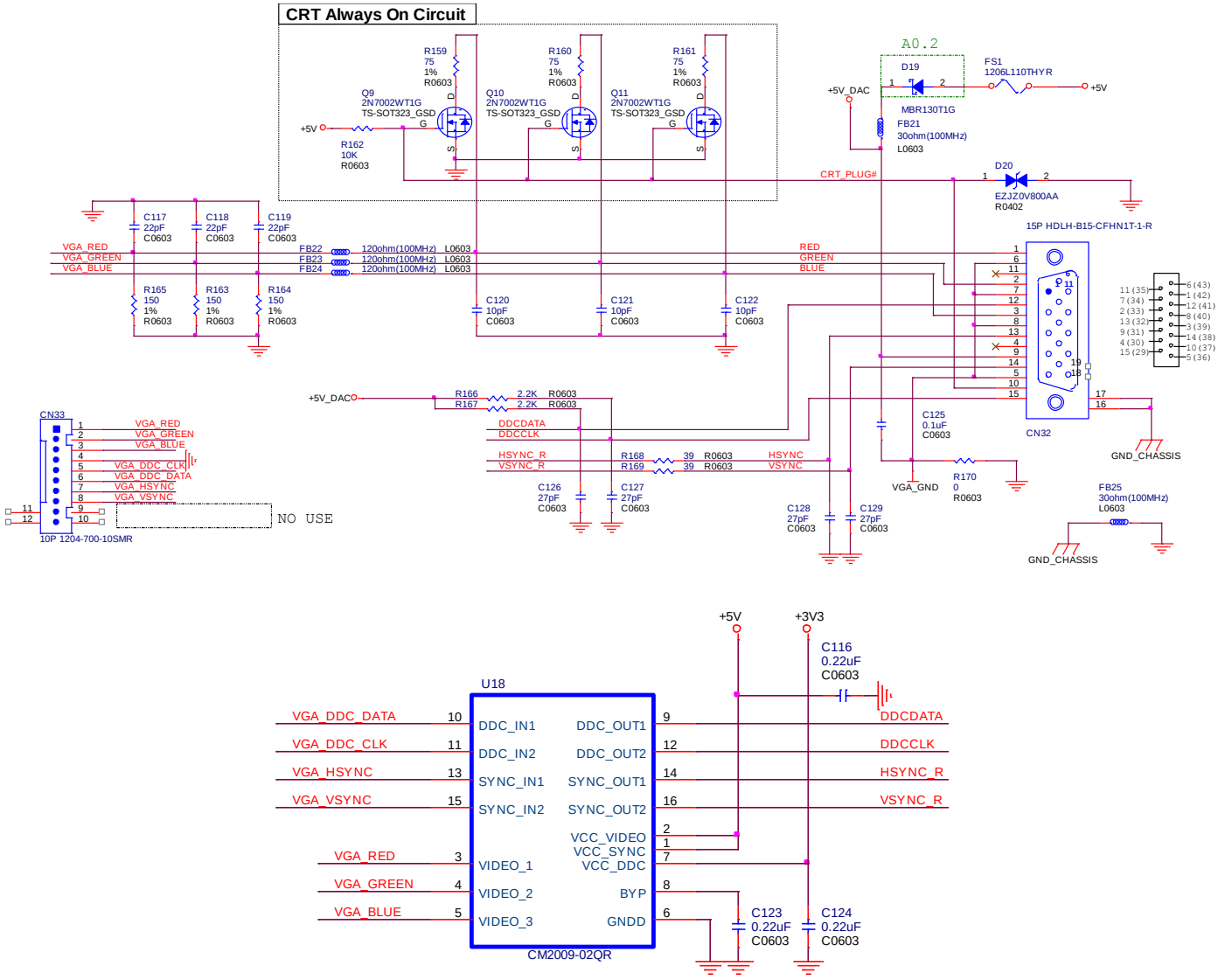
Figure 2-14 Battery Schematic



2.10.2. CRT schematic

MXM connector doesn't define CRT signals. So it (AQ7-LN) needs to have an extra cable to connect between Q7 CPU module and ECB-970.

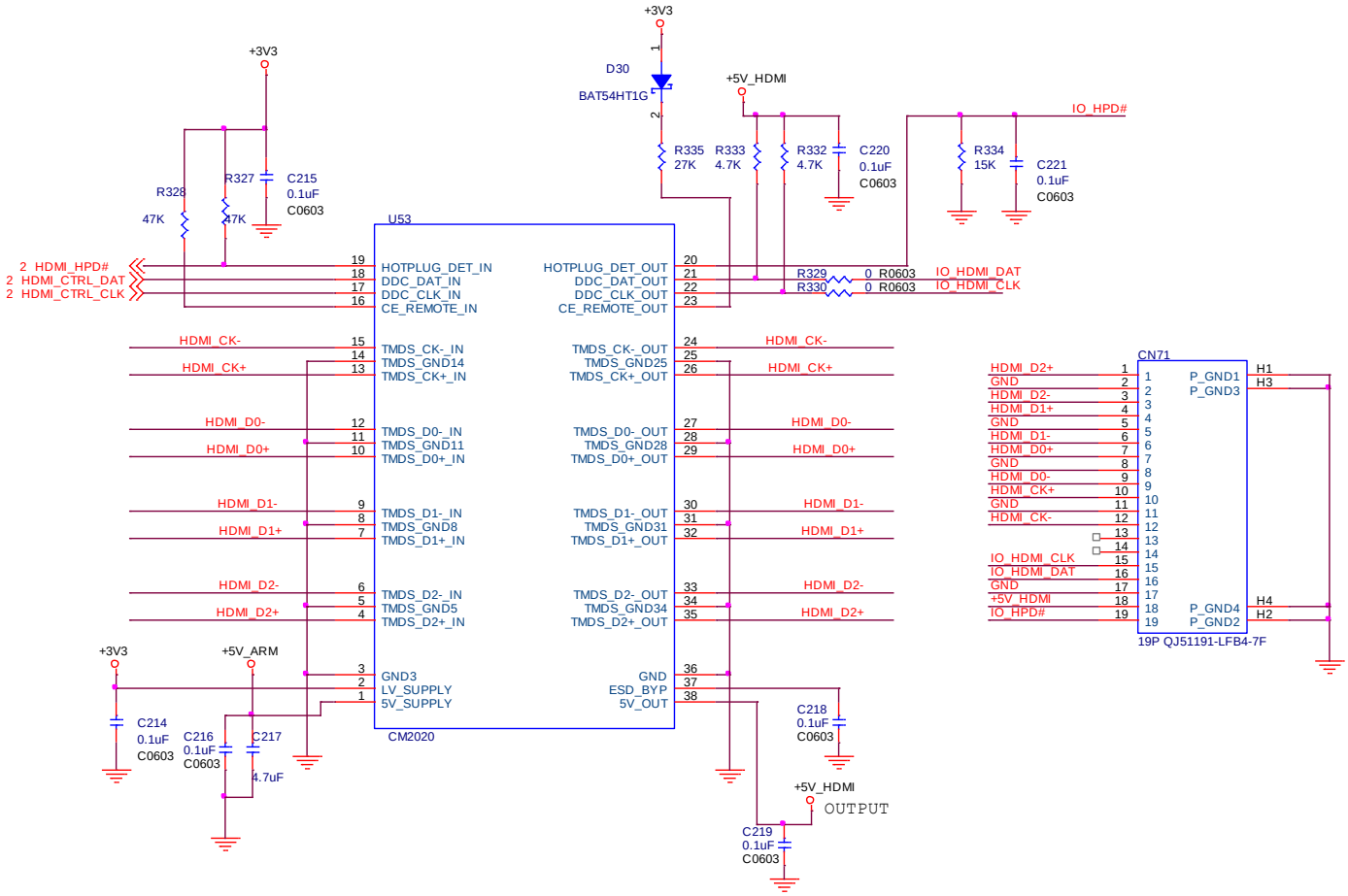
Figure 2-15 CRT Schematic



2.10.3. HDMI schematic

The following is for AQ7-iMX6 HDMI. AQ7-iMX6 doesn't need the external HDMI level shifter. CM2020 provides ESD protection and DDC level shifter.

Figure 2-16 AQ7-IMX6 HDMI Schematic



The following is for AQ7-LN and AQ7-BT HDMI level shifter design.

Figure 2-17 AQ7-BT HDMI level shifter schematic

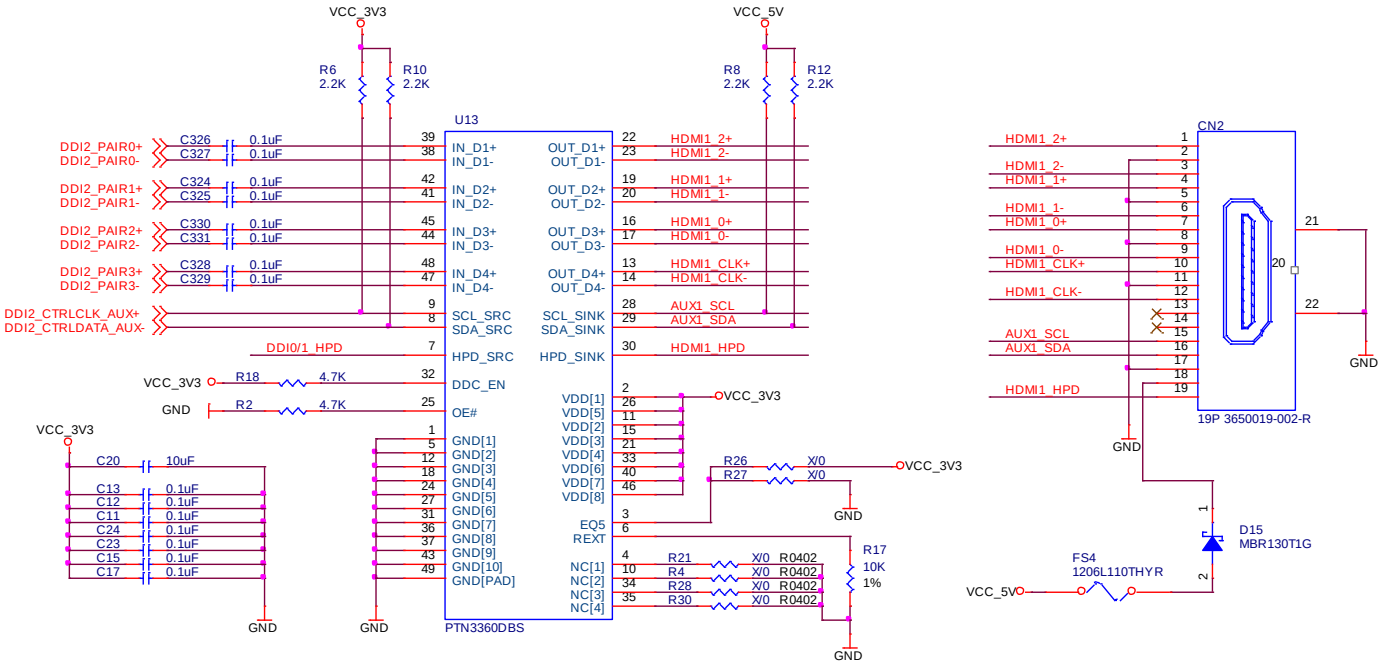
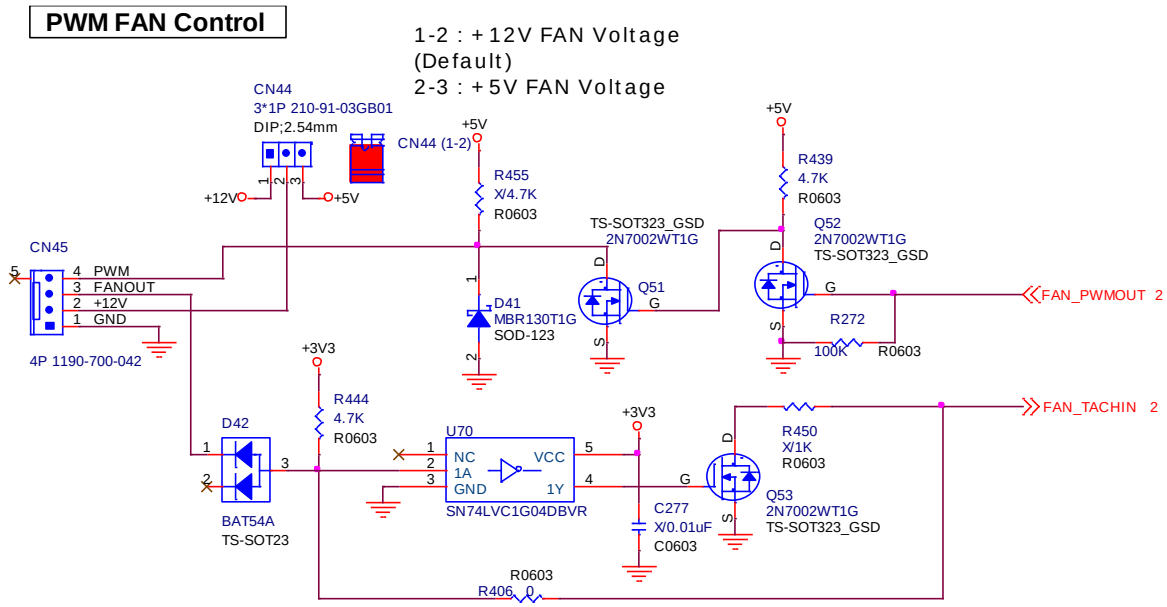


Table 8 HDMI layout guide

Parameter	Definition
Differential impedance target	95Ω ± 15%
Trace width (W)	4 mils (Dependent on stack)
Trace spacing (S) (intra-pair)	6 mils (Dependent on stack)
Trace spacing (S) (inter-pair)	20 mils
Reference plane	GND referencing preferred GND stitching vias required next to signal vias
Length matching within differential pair (intra-pair)	Max. 5 mils
Length matching between clock and data pairs	Max. 20 mils
Signal length (L) (carrier board)	Max. 5 inches

2.10.4. FAN schematic

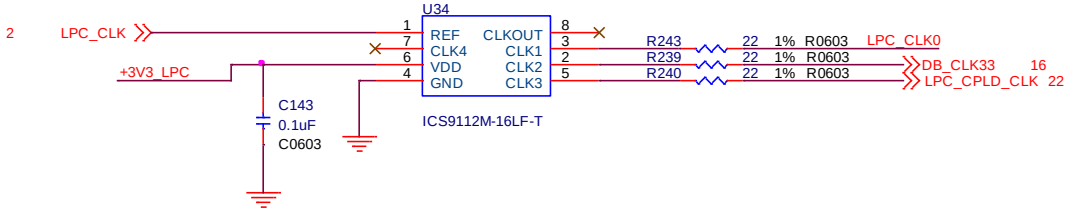
Figure 2-18 FAN Schematic



2.10.5. Clock buffer schematic

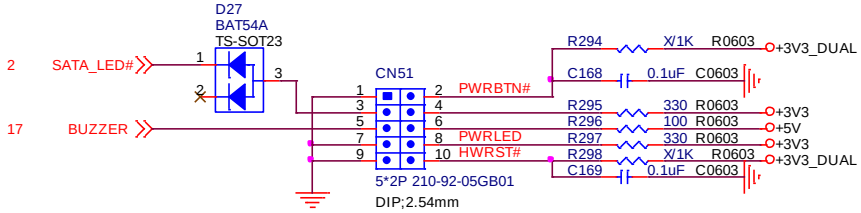
Clock buffer is for AQ7-LN and AQ7-BT that support LPC bus.

Figure 2-19 Clock buffer Schematic



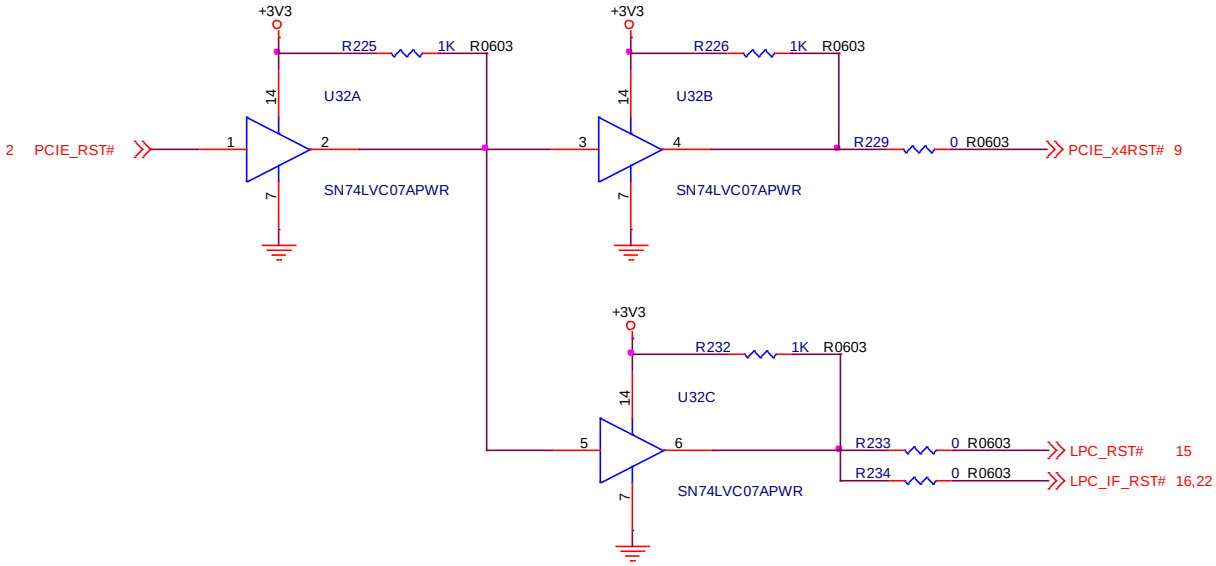
2.10.6. Front Panel schematic

Figure 2-20 Front panel Schematic



2.10.7. Reset Buffer schematic

Figure 2-21 Reset buffer schematic



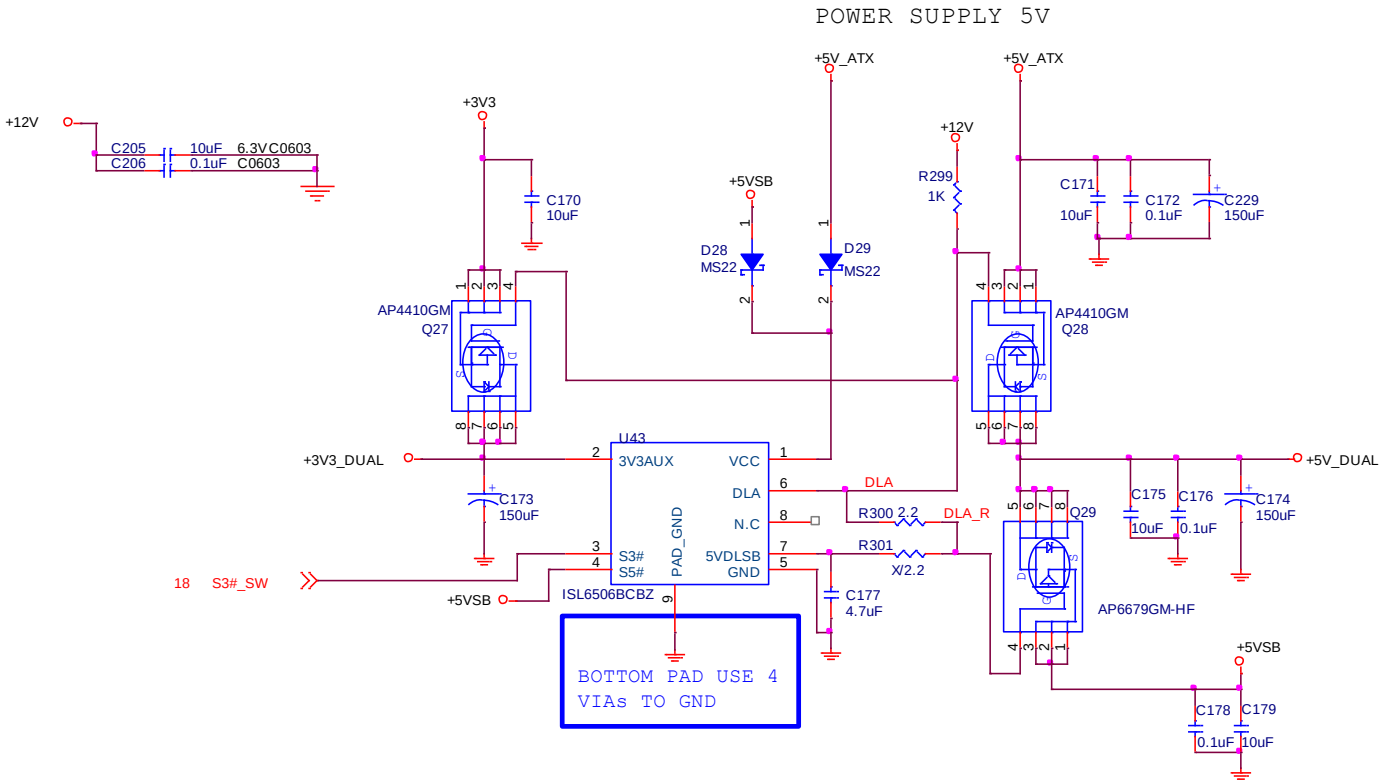
2.11. Power solution

The following is the application schematic in ECB-970.

2.11.1. +5V_DUAL power schematic

The ISL6506B is for +5V_DUAL and +3V3_DUAL power controller.

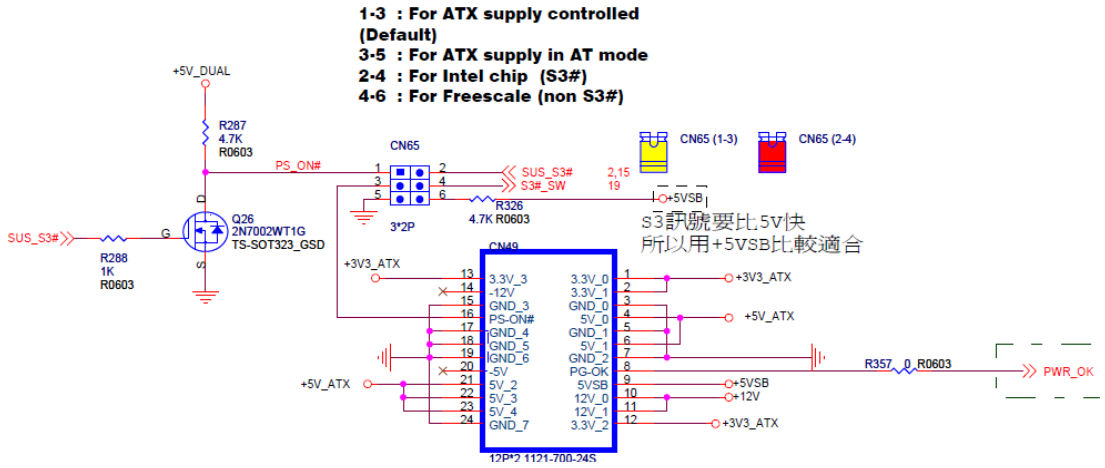
Figure 2-22 +5V_DUAL, +3V3_DUAL power schematic



2.11.2. ATX power schematic

AQ7-iMX6 needs to set CN65 pin 3-5 and 4-6 on to keep the power supply always on.

Figure 2-23 ATX power schematic



Chapter 3 Mechanical and Heat spreader consideration

3.1. Q7 CPU module mechanical drawing

Figure 3-1 Q7 CPU module mechanical drawing

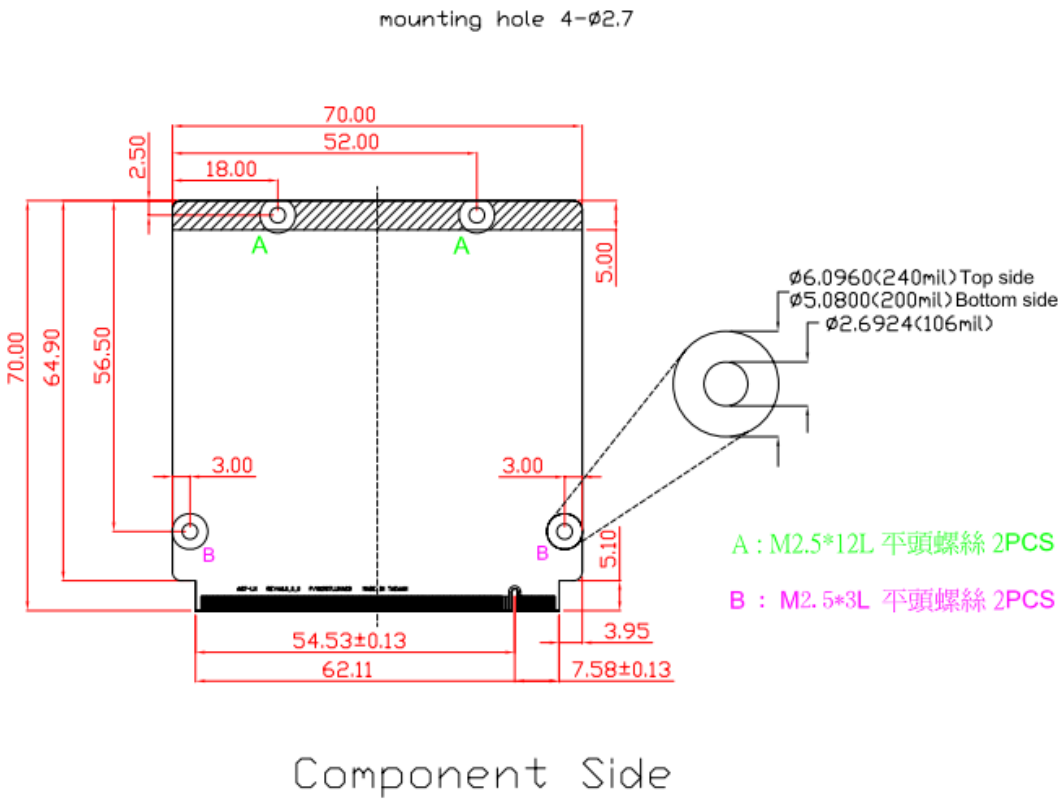
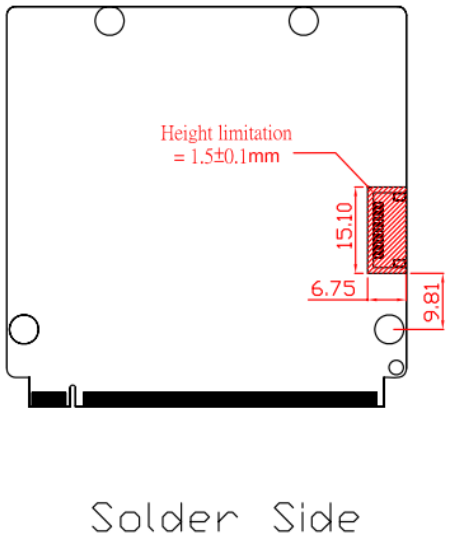


Figure 3-1 shows the Q7 CPU module mechanical drawing.

Figure 3-2 AQ7-LN CPU module height limitation on solder side



AQ7-LN A/B 1.0 solder side has a connector for CRT function. The height of connector is 2.9 ± 0.25 mm. We suggest the height limitation on carrier board in this area is 1.5 ± 0.1 mm instead of 2.2 ± 0.1 mm. AQ7-LN C/D 1.0 won't have this limitation.

3.2. Recommendation for height limitation

Figure 3-3 Height limitation on carrier board

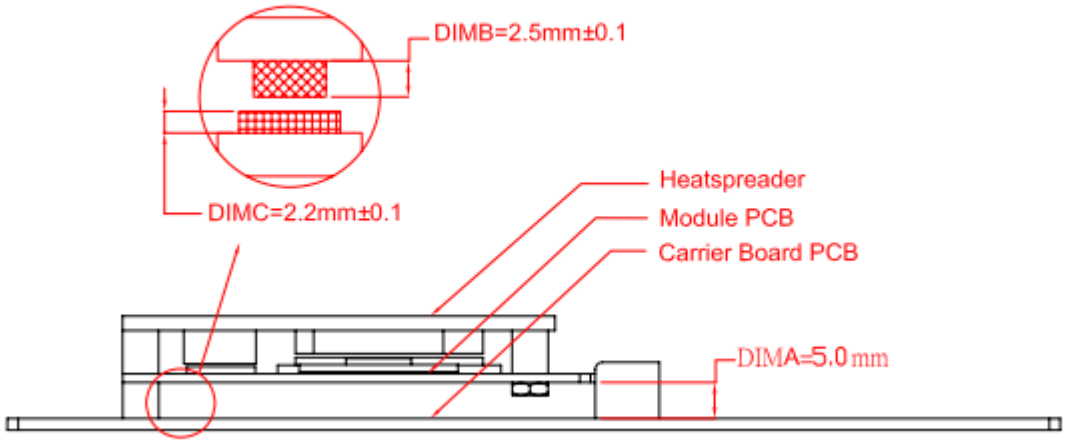


Figure 3-3 is the height limitation drawing. The height of Q7 carrier board (top side) cannot exceed 2.2 ± 0.1 mm.

3.3. Heat spreader for Q7 module

Figure 3-4 Heat spreader drawing

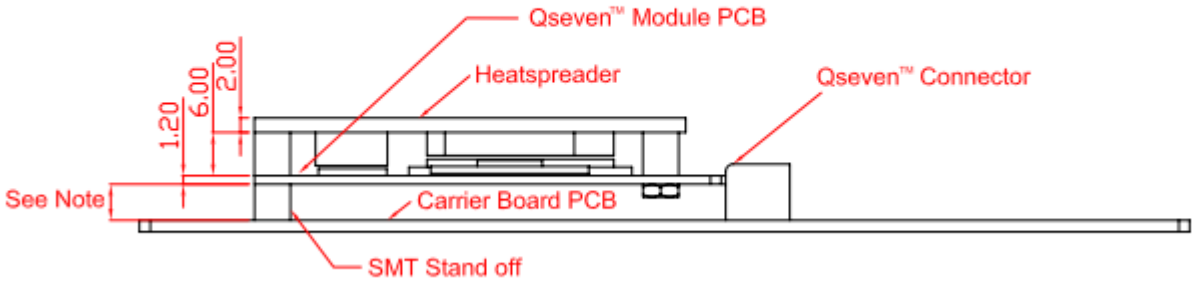
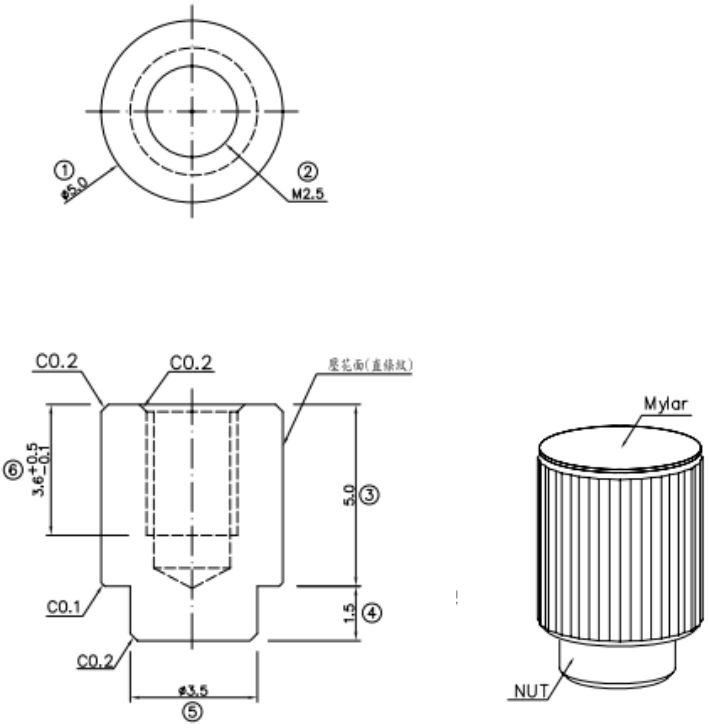
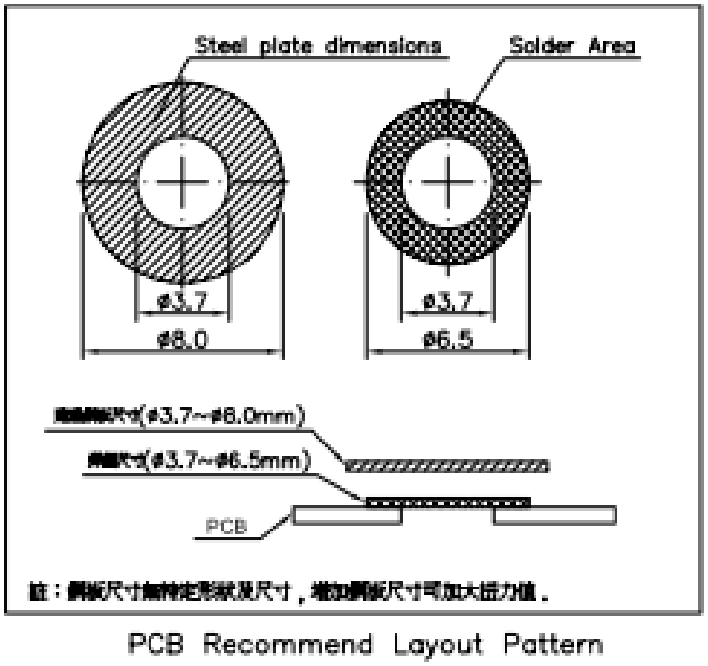


Figure 3-4 shows the assembly drawing of heat spreader for AQ7-LN and ECB-970 carrier board.

3.4. Stud for carrier board

Figure 3-5 Stud drawing





PCB Recommend Layout Pattern

Figure 3-5 shows the drawing of stud using on the ECB-970 carrier board. It also shows the PCB recommend layout pattern on the carrier board.

Chapter 4 MXM Connector Pin Define

4.1. MXM 1-99 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
1	GND	P		GND	
3	GBE_MDI3-	I/O		MDI differential pair 3	
5	GBE_MDI3+	I/O		MDI differential pair 3	
7	GBE_LINK100#	O		LAN 100Mbit/sec link indicator	
9	GBE_MDI1-	I/O		MDI differential pair 1	
11	GBE_MDI1+	I/O		MDI differential pair 1	
13	GBE_LINK#	O		LAN link indicator	
15	GBE_CTREF	O		LAN: reference voltage for magnetic center tap	
17	WAKE#	I		External system wake event	
19	GPO0	O		GPO0	SUS_STAT#
21	SLP_BTN# / GPII1	I		Sleep button	GPII1
23	GND	P		GND	
25	GND	P		GND	
27	BATLOW# / GPII2	I		Battery low: It's an input from battery to indicate that there is insufficient power to boot the system. This signal can also be configured as a GPIO.	GPII2
29	SATA0_TX+	O		SATA TX pair 0	
31	SATA0_TX-	O		SATA TX pair 0	
33	SATA_ACT#	O		SATA LED	
35	SATA0_RX+	I		SATA RX pair 0	
37	SATA0_RX-	I		SATA RX pair 0	
39	GND	P		GND	
41	BIOS_DISABLE# / BOOT_ALT#	I		Module BIOS disable. Pull-low to disable module's BIOS.	BOOT_ALT#
43	SDIO_CD#	I/O		SD card detect	NC
45	SDIO_CMD	I/O		SD command	NC
47	SDIO_PWR#	O		SD power enable	NC
49	SDIO_DAT0	I/O		SD data line	NC
51	SDIO_DAT2	I/O		SD data line	NC
53	RSVD	I/O		NC	SDIO_DAT4
55	RSVD	I/O		NC	SDIO_DAT6
57	GND	P		GND	

59	HDA_SYNC / I2S_WS	O		HD SYNC	I2S_WS
61	HDA_RST# / I2S_RST#	O		HD reset	I2S_RST#
63	HDA_BITCLK / I2S_CLK	O		HD clock	I2S_CLK
65	HDA_SDI / I2S_SDI	I		HD data input	I2S_SDI
67	HDA_SDO / I2S_SDO	O		HD data output	I2S_SDO
69	THRM#	I		Thermal alarm	
71	THRMTRIP#	O		Thermal trip	
73	GND	P		GND	
75	USB_P7- / USB_SSTX0-	I/O		USB port 7	USB_SSTX0-
77	USB_P7+ / USB_SSTX0+	I/O		USB port 7	USB_SSTX0+
79	USB_6_7_OC#	I		USB over current for port 6,7	
81	USB_P5- / USB_SSTX2-	I/O		USB port 5	USB_SSTX2-
83	USB_P5+ / USB_SSTX2+	I/O		USB port 5	USB_SSTX2+
85	USB_2_3_OC#	I		USB over current for port 2,3	
87	USB_P3-	I/O		USB port 3	
89	USB_P3+	I/O		USB port 3	
91	USB_VBUS	I		NC	USB_VBUS
93	USB_P1-	I/O		USB port 1	USB_OTG-
95	USB_P1+	I/O		USB port 1	USB_OTG+
97	GND	P		GND	
99	eDP0_TX0+ / LVDS_A0+	O		LVDS primary differential pair 0	eDP0_TX0+

4.2. MXM 2-100 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
2	GND	P		GND	
4	GBE_MDI2-	I/O		MDI differential pair 2	
6	GBE_MDI2+	I/O		MDI differential pair 2	
8	GBE_LINK1000#	O		LAN 1000Mbit/sec link indicator	
10	GBE_MDI0-	I/O		MDI differential pair 0	
12	GBE_MDI0+	I/O		MDI differential pair 0	
14	GBE_ACT#	O		LAN activity indicator	
16	SUS_S5#	O		S5 state	
18	SUS_S3#	O		S3 state	
20	PWRBTN#	I	Pull-up 10K	Power button	
22	LID_BTN# /GPII0	I	Pull-up 10K	LID button	GPII0
24	GND	P		GND	
26	PWGIN	I	Pull-up 10K	All power rails on carrier board are ready	
28	RSTBTN#	I	Pull-up 10K	Reset button	
30	SATA1_TX+	O		SATA TX pair 1	
32	SATA1_TX-	O		SATA TX pair 1	
34	GND	P		GND	
36	SATA1_RX+	I		SATA RX pair 0	
38	SATA1_RX-	I		SATA RX pair 0	
40	GND	P		GND	
42	SDIO_CLK	O		SD clock	NC
44	RSVD	O		NC	
46	SDIO_WP	I/O		SD write protect	NC
48	SDIO_DAT1	I/O		SD data line	NC
50	SDIO_DAT3	I/O		SD data line	NC
52	RSVD	I/O		NC	SDIO_DAT5
54	RSVD	I/O		NC	SDIO_DAT7
56	USB_OTG_PEN	O		USB Power enable for USB Port 1	
58	GND	P		GND	
60	SMB_CLK / GP1_I2C_CLK	I/O	Pull-up 2.2K	SM Bus clock	GP1_I2C_CLK
62	SMB_DAT / GP1_I2C_DAT	I/O	Pull-up 2.2K	SM Bus data	GP1_I2C_DAT
64	SMB_ALERT#	I/O	Pull-up 10K	SM Bus alert	

66	GP0_I2C_CLK	I/O	Pull-up 2.2K	GP0_I2C_CLK	
68	GP0_I2C_DAT	I/O	Pull-up 2.2K	GP0_I2C_DAT	
70	WDTRIG#	I	Pull-up 4.7K	Watchdog trigger signal	
72	WDOUT	O	Pull-up 1K	Watchdog output event	
74	GND	P		GND	
76	USB_P6- / USB_SSRX0-	I/O		USB port 6	USB_SSRX0-
78	USB_P6+ / USB_SSRX0+	I/O		USB port 6	USB_SSRX0+
80	USB_4_5_OC#	I	Pull-up 10K	USB over current for port 4,5	
82	USB_P4- / USB_SSRX2-	I/O		USB port 4	USB_SSRX2-
84	USB_P4+ USB_SSRX2+	I/O		USB port 4	USB_SSRX2+
86	USB_0_1_OC#	I	Pull-up 10K	USB over current for port 0,1	
88	USB_P2-	I/O		USB port 2	
90	USB_P2+	I/O		USB port 2	
92	USB_ID	I		USB client mode setting	NC
94	USB_P0-	I/O		USB port 0	
96	USB_P0+	I/O		USB port 0	
98	GND	P		GND	
100	eDP1_TX0+ / LVDS_B0+	O		eDP1_TX0+	LVDS_B0+

4.3. MXM 101-199 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
101	eDP0_TX0- / LVDS_A0-	O		LVDS primary differential pair 0	eDP0_TX0-
103	eDP0_TX1+ / LVDS_A1+	O		LVDS primary differential pair 1	eDP0_TX1+
105	eDP0_TX1- / LVDS_A1-	O		LVDS primary differential pair 1	eDP0_TX1-
107	eDP0_TX2+ / LVDS_A2+	O		LVDS primary differential pair 2	eDP0_TX2+
109	eDP0_TX2- / LVDS_A2-	O		LVDS primary differential pair 2	eDP0_TX2-
111	LVDS_PPEN	O	Pull-dn 100K	LVDS panel power enable	
113	eDP0_TX3+ / LVDS_A3+	O		LVDS primary differential pair 3	eDP0_TX3+
115	eDP0_TX3- / LVDS_A3-	O		LVDS primary differential pair 3	eDP0_TX3-
117	GND	P		GND	
119	eDP0_AUX+ / LVDS_A_CLK+	O		LVDS primary differential pair clock	eDP0_AUX+
121	eDP0_AUX- / LVDS_A_CLK-	O		LVDS primary differential pair clock	
123	LVDS_BLT_CTRL / GP_PWM_OUT0	O		LVDS backlight brightness PWM control	GP_PWM_OUT0
125	GP2_I2C_DAT / LVDS_DID_DAT	I/O	Pull-up 8.2K	GP2_I2C_DAT	LVDS EDID data
127	GP2_I2C_CLK / LVDS_DID_CLK	I/O	Pull-up 8.2K	GP2_I2C_CLK	LVDS_DID_CLK
129	CAN0_TX	O		CAN bus TX	NC
131	DP_LANE3+ / TMDS_CLK+	O		DP_LANE3+	TMDS_CLK+
133	DP_LANE3- / TMDS_CLK-	O		DP_LANE3-	TMDS_CLK-
135	GND	P		GND	
137	DP_LANE1+ / TMDS_LANE1+	O		DP_LANE1+	TMDS_LANE1+
139	DP_LANE1-	O		DP_LANE1-	TMDS_LANE1-

	/ TMDS_LANE1-				
141	GND	P		GND	
143	DP_LANE2+ / TMDS_LANE0+	O		DP_LANE2+	TMDS_LANE0+
145	DP_LANE2- / TMDS_LANE0-	O		DP_LANE2-	TMDS_LANE0-
147	GND	P		GND	
149	DP_LANE0+ / TMDS_LANE2+	O		DP_LANE0+	TMDS_LANE2+
151	DP_LANE0- / TMDS_LANE2-	O		DP_LANE0-	TMDS_LANE2-
153	HDMI_HPD#	I		HDMI_HPD#	
155	PCIE_CLK_REF+	O		PCI Express reference clock	
157	PCIE_CLK_REF-	O		PCI Express reference clock	
159	GND	P		GND	
161	PCIE3_TX+	O		PCI Express channel 3	
163	PCIE3_TX-	O		PCI Express channel 3	
165	GND	P		GND	
167	PCIE2_TX+	O		PCI Express channel 2	
169	PCIE2_TX-	O		PCI Express channel 2	
171	UART0_TX	O		UART0 TX	
173	PCIE1_TX+	O		PCI Express channel 1	
175	PCIE1_TX-	O		PCI Express channel 1	
177	UART0_RX	I		UART0 RX	
179	PCIE0_TX+	O		PCI Express channel 0	
181	PCIE0_TX-	O		PCI Express channel 0	
183	GND	P		GND	
185	LPC_AD0 / GPIO0	I/O		LPC Multiplexed command, address, data	GPIO0
187	LPC_AD2 / GPIO2	I/O		LPC Multiplexed command, address, data	GPIO2
189	LPC_CLK / GPIO4	O		LPC clock	GPIO4
191	SERIRQ / GPIO6	I/O	Pull-up 10K	Serial interrupt request	GPIO6
193	VCC_RTC	P		3.3V supply for the RTC cell	
195	FAN_TACHOIN / GP_TIMER_IN	I		Primary is for fan tachometer input. It can be used as Timer input	GP_TIMER_IN
197	GND	P		GND	

199	SPI_MOSI	O		SPI master out/slave in	SPI_SI

4.4. MXM 102-200 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
102	eDP1_TX0- / LVDS_B0-	O		eDP1_TX0-	LVDS_B0-
104	eDP1_TX1+ / LVDS_B1+	O		eDP1_TX1+	LVDS_B1+
106	eDP1_TX1- / LVDS_B1-	O		eDP1_TX1-	LVDS_B1-
108	eDP1_TX2+ / LVDS_B2+	O		eDP1_TX2+	LVDS_B2+
110	eDP1_TX2- / LVDS_B2-	O		eDP1_TX2-	LVDS_B2-
112	LVDS_BLEN	O	Pull-dn 100K	LVDS backlight enable	
114	eDP1_TX3+ / LVDS_B3+	O		eDP1_TX3+	LVDS_B3+
116	eDP1_TX3- / LVDS_B3-	O		eDP1_TX3-	LVDS_B3-
118	GND	P		GND	
120	eDP1_AUX+ / LVDS_B_CLK+	O		eDP1_AUX+	LVDS_B_CLK+
122	eDP1_AUX- / LVDS_B_CLK-	O		eDP1_AUX-	LVDS_B_CLK-
124	GP_1-Wire_Bus / HDMI_CEC			GP_1-Wire_Bus	HDMI_CEC
126	eDP0_HPD# / LVDS_BLC_DAT	I/O		eDP0_HPD#	LVDS_BLC_DAT
128	eDP1_HPD# / LVDS_BLC_CLK	I/O		eDP1_HPD#	LVDS_BLC_CLK
130	CAN0_RX	I		CAN bus RX	NC
132	USB_SSTX1-	I		USB_SSTX1-	NC
134	USB_SSTX1+	I		USB_SSTX1+	NC
136	GND	P		GND	
138	DP_AUX+	I		DP AUX differential pair	NC
140	DP_AUX-	I		DP AUX differential pair	NC
142	GND	P		GND	

144	USB_SSRX1-	I		USB_SSRX1-	NC
146	USB_SSRX1+	I		USB_SSRX1+	NC
148	GND	P		GND	
150	HDMI_CTRL_DAT	I/O		DDC data for HDMI	NC
152	HDMI_CTRL_CLK	I/O		DDC clock for HDMI	NC
154	DP_HPD#	I		Hot plug detection for display port	NC
156	PCIE_WAKE#	I	Pull-up 1K	PCI Express wake event	
158	PCIE_RST#	O	Pull-up 1K	PCI Express reset	
160	GND	P		GND	
162	PCIE3_RX+	I		PCI Express channel 3	NC
164	PCIE3_RX-	I		PCI Express channel 3	NC
166	GND	P		GND	
168	PCIE2_RX+	I		PCI Express channel 2	NC
170	PCIE2_RX-	I		PCI Express channel 2	NC
172	UART0_RTS#	O		UART0 RTS#	NC
174	PCIE1_RX+	I		PCI Express channel 1	
176	PCIE1_RX-	I		PCI Express channel 1	
178	UART0_CTS#	I		UART0 CTS#	NC
180	PCIE0_RX+	I		PCI Express channel 0	
182	PCIE0_RX-	I		PCI Express channel 0	
184	GND	P		GND	
186	LPC_AD1 / GPIO1	I/O		LPC Multiplexed command, address, data	GPIO1
188	LPC_AD3 / GPIO3	I/O		LPC Multiplexed command, address, data	GPIO3
190	LPC_FRAME# / GPIO5	O		LPC Frame	GPIO5
192	LPC_LDRQ# / GPIO7	I		LPC Serial DMA/Master Request Input	GPIO7
194	SPKR / GP_PWM_OUT2	O		Speaker	GP PWM Output
196	FAN_PWMOUT / GP_PWM_OUT1	O		Primary for fan speed control. It can be used as PWM output	GP PWM Output
198	GND	P		GND	
200	SPI_CS0#	O		SPI chip select 0	

4.5. MXM 201-229 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
201	SPI_MISO	I		SPI master in/slave out	SPI_SO
203	SPI_SCK	O		SPI clock	
205	VCC_5V_SB	P		+5V Standby power	
207	MFG_NC0			NC	TCK_M
209	MFG_NC1			NC	TMS_M
211	NC	P		NC	+5V
213	NC	P		NC	+5V
215	NC	P		NC	+5V
217	NC	P		NC	+5V
219	VCC	P		+5V	
221	VCC	P		+5V	
223	VCC	P		+5V	
225	VCC	P		+5V	
227	VCC	P		+5V	
229	VCC	P		+5V	

4.6. MXM 202-230 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
202	SPI_CS1#	O		SPI chip select 1	NC
204	MFG_NC4			NC	NC
206	VCC_5V_SB	P		+5V Standby power	NC
208	MFG_NC2			NC	TDO_M
210	MFG_NC3			NC	TDI_M
212	NC	P		NC	+5V
214	NC	P		NC	+5V
216	NC	P		NC	+5V
218	NC	P		NC	+5V
220	VCC	P		+5V	
222	VCC	P		+5V	
224	VCC	P		+5V	
226	VCC	P		+5V	
228	VCC	P		+5V	
230	VCC	P		+5V	

4.7. CN7 pin description

Pin	Signal	I/O	Pull-Up or Dn in Q7 module	Pin Description	Optional Description
1	VGA_R	O	Pull-dn 150R	Red analog video output	
2	VGA_G	O	Pull-dn 150R	Green analog video output	
3	VGA_B	O	Pull-dn 150R	Blue analog video output	
4	GND	P		Ground	
5	DDC_SMBCLK	I/O	Pull-up 6.8K	CRT DDC clock	
6	DDC_SMBDAT	I/O	Pull-up 6.8K	CRT DDC data	
7	VGA_HSYNC	O		CRT HSYNC	
8	VGA_VSYNC	O		CRT VSYNC	
9	SMI#	I	Pull-up 10K	SMI#	
10	SCI	I		SCI	

Chapter 5 Change History

Version	Change Description	Note
0.3	Chapter 4 Appendix update	
0.4	Add AQ7-iMX6 support for I2S (Audio) and HDMI. Add ECB-970 support, remove ECB-930G support	
0.5	Chapter 2.4, add LAN connector spec for AQ7- LN, AQ7-BT and AQ7-iMX6.	
0.6	Chapter 2.10.3, add Figure 2-16 AQ7-BT HDMI schematic.	
1.0	Chapter 2.6.2 adds USB OTG for AQ7- iMX6. Chapter 2.10.3 adds HDMI description for AQ7- iMX6. Chapter 2.11.2 adds ATX power schematic for AQ7- iMX6. Chapter 4 update pin-out	Version 2.1 (2016-2-25)
1.0.1	Add Chapter 1.2 section with AT and ATX power state and sequence Add AQ7-APL and AQ7-BT pinout in Appendix I, II, III	2017.04.01

Appendix I: AQ7-APL Module Pin Out (Qseven 2.1)

AQ7-APL Pin-Out (Qseven 2.1 compliance)

Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark	Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark
1	GND	GND		2	GND	GND	
3	GBE_MDI3-	GBE_MDI3-		4	GBE_MDI2-	GBE_MDI2-	
5	GBE_MDI3+	GBE_MDI3+		6	GBE_MDI2+	GBE_MDI2+	
7	GBE_LINK100#	GBE_LINK100#		8	GBE_LINK1000#	GBE_LINK1000#	
9	GBE_MDI1-	GBE_MDI1-		10	GBE_MDI0-	GBE_MDI0-	
11	GBE_MDI1+	GBE_MDI1+		12	GBE_MDI0+	GBE_MDI0+	
13	GBE_LINK#	GBE_LINK#		14	GBE_ACT#	GBE_ACT#	
15	GBE_CTREF	GBE_CTREF		16	SUS_S5#	SUS_S5#	
17	WAKE#	WAKE#		18	SUS_S3#	SUS_S3#	
19	GPO0	NC	AQ7-APL no support GPO0	20	PWRBTN#	PWRBTN#	
21	SLP_BTN# / GPII1	SLP_BTN#	AQ7-APL no support GPII1	22	LID_BTN# / GPII0	LID_BTN#	AQ7-APL no support GPII0
23	GND	GND		24	GND	GND	
25	GND	GND		26	PWGIN	PWGIN	
27	BATLOW# / GPII2	BATLOW#	AQ7-APL no support GPII2	28	RSTBTN#	RSTBTN#	
29	SATA0_TX+	SATA0_TX+		30	SATA1_TX+	SATA1_TX+	
31	SATA0_TX-	SATA0_TX-		32	SATA1_TX-	SATA1_TX-	
33	SATA_ACT#	SATA_ACT#		34	GND	GND	
35	SATA0_RX+	SATA0_RX+		36	SATA1_RX+	SATA1_RX+	
37	SATA0_RX-	SATA0_RX-		38	SATA1_RX-	SATA1_RX-	
39	GND	GND		40	GND	GND	
41	BIOS_DISABLE# / BOOT_ALT#	BIOS_DISABLE#	AQ7-APL no support BOOT_ALT#	42	SDIO_CLK#	SDIO_CLK#	
43	SDIO_CD#	SDIO_CD#		44	reserved	reserved	
45	SDIO_CMD	SDIO_CMD		46	SDIO_WP	SDIO_WP	
47	SDIO_PWR#	SDIO_PWR#		48	SDIO_DAT1	SDIO_DAT1	
49	SDIO_DAT0	SDIO_DAT0		50	SDIO_DAT3	SDIO_DAT3	
51	SDIO_DAT2	SDIO_DAT2		52	reserved	reserved	
53	reserved	reserved		54	reserved	reserved	
55	reserved	reserved		56	USB_OTG_PEN	NC	AQ7-APL no support USB_OTG_PEN
57	GND	GND		58	GND	GND	
59	HDA_SYNC / I2S_WS	HDA_SYNC		60	SMB_CLK / GP1_I2C_CLK	SMB_CLK	SOC,
61	HDA_RST# / I2S_RST#	HDA_RST#	AQ7-APL no support I2S_RST#	62	SMB_DAT / GP1_I2C_DAT	SMB_DAT	SOC,
63	HDA_BITCLK / I2S_CLK	HDA_BITCLK	AQ7-APL no support I2S_CLK	64	SMB_ALERT#	SMB_ALERT#	
65	HDA_SDI / I2S_SDI	HDA_SDI	AQ7-APL no support I2S_SDI	66	GP0_I2C_CLK	GP0_I2C_CLK	EC
67	HDA_SDO / I2S_SDO	HDA_SDO	AQ7-APL no support I2S_SDO	68	GP0_I2C_DAT	GP0_I2C_DAT	EC

Connector Pinout Description

Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark	Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark
69	THRM#	THRM#		70	WDTRIG#	NC	AQ7-APL no support WDTRIG#
71	THRMTRIP#	THRMTRIP#		72	WDOUT	WDOUT	
73	GND	GND		74	GND	GND	
75	USB_P7- / USB_SSTX0-	USB_SSTX0-	AQ7-APL no support USB_P7-	76	USB_P6- / USB_SSRX0-	USB_SSRX0-	AQ7-APL no support USB_P6-
77	USB_P7+ / USB_SSTX0+	USB_SSTX0+	AQ7-APL no support USB_P7+	78	USB_P6+ / USB_SSRX0+	USB_SSRX0+	AQ7-APL no support USB_P6+
79	USB_6_7_OC#	USB_6_7_OC#		80	USB_4_5_OC#	USB_4_5_OC#	
81	USB_P5- / USB_SSTX2-	USB_P5-	AQ7-APL no support USB_SSTX2-	82	USB_P4- / USB_SSRX2-	USB_P4-	AQ7-APL no support USB_SSRX2-
83	USB_P5+ / USB_SSTX2+	USB_P5+	AQ7-APL no support USB_SSTX2+	84	USB_P4+ / USB_SSRX2+	USB_P4+	AQ7-APL no support USB_SSRX2+
85	USB_2_3_OC#	USB_2_3_OC#		86	USB_0_1_OC#	USB_0_1_OC#	
87	USB_P3-	USB_P3-		88	USB_P2-	USB_P2-	
89	USB_P3+	USB_P3+		90	USB_P2+	USB_P2+	
91	USB_VBUS	NC		92	USB_ID	NC	
93	USB_P1-	USB_P1-		94	USB_P0-	USB_P0-	
95	USB_P1+	USB_P1+		96	USB_P0+	USB_P0+	
97	GND	GND		98	GND	GND	
99	eDP0_TX0+ / LVDS_A0+	LVDS_A0+ / (eDP0_TX0+)	Option function is Gray font	100	eDP1_TX0+ / LVDS_B0+	LVDS_B0+	AQ7-APL no support eDP1_TX0+
101	eDP0_TX0- / LVDS_A0-	LVDS_A0- / (eDP0_TX0-)	Option function is Gray font	102	eDP1_TX0- / LVDS_B0-	LVDS_B0-	AQ7-APL no support eDP1_TX0-
103	eDP0_TX1+ / LVDS_A1+	LVDS_A1+ / (eDP0_TX1+)	Option function is Gray font	104	eDP1_TX1+ / LVDS_B1+	LVDS_B1+	AQ7-APL no support eDP1_TX1+
105	eDP0_TX1- / LVDS_A1-	LVDS_A1- / eDP0_TX1-	Option function is Gray font	106	eDP1_TX1- / LVDS_B1-	LVDS_B1-	AQ7-APL no support eDP1_TX1-
107	eDP0_TX2+ / LVDS_A2+	LVDS_A2+ / eDP0_TX2+	Option function is Gray font	108	eDP1_TX2+ / LVDS_B2+	LVDS_B2+	AQ7-APL no support eDP1_TX2+
109	eDP0_TX2- / LVDS_A2-	LVDS_A2- / (eDP0_TX2-)	Option function is Gray font	110	eDP1_TX2- / LVDS_B2-	LVDS_B2-	AQ7-APL no support eDP1_TX2-
111	LVDS_PPEN	LVDS_PPEN		112	LVDS_BLEN	LVDS_BLEN	
113	eDP0_TX3+ / LVDS_A3+	LVDS_A3+ / (eDP0_TX3+)	Option function is Gray font	114	eDP1_TX3+ / LVDS_B3+	LVDS_B3+	AQ7-APL no support eDP1_TX3+
115	eDP0_TX3- / LVDS_A3-	LVDS_A3- / (eDP0_TX3-)	Option function is Gray font	116	eDP1_TX3- / LVDS_B3-	LVDS_B3-	AQ7-APL no support eDP1_TX3-
117	GND	GND		118	GND	GND	
119	eDP0_AUX+ / LVDS_A_CLK+	LVDS_A_CLK+ / (eDP0_AUX+)	Option function is Gray font	120	eDP1_AUX+ / LVDS_B_CLK+	LVDS_B_CLK+	AQ7-APL no support eDP1_AUX+
121	eDP0_AUX- / LVDS_A_CLK-	LVDS_A_CLK- / (eDP0_AUX-)	Option function is Gray font	122	eDP1_AUX- / LVDS_B_CLK-	LVDS_B_CLK-	AQ7-APL no support eDP1_AUX-
123	LVDS_BLT_CTRL / GP_PWM_OUT0	LVDS_BLT_CTRL	AQ7-APL no support GP_PWM_OUT0	124	GP_1-Wire_Bus / HDMI_CEC	NC	AQ7-APL no support GP_1-Wire_Bus / HDMI_CEC
125	GP2_I2C_DAT / LVDS_DID_DAT	LVDS_DID_DAT	AQ7-APL no support GP2_I2C_DAT	126	eDP0_HPD# / LVDS_BLC_DAT	eDP0_HPD#	AQ7-APL no support LVDS_BLC_DAT
127	GP2_I2C_CLK / LVDS_DID_CLK	LVDS_DID_CLK	AQ7-APL no support GP2_I2C_CLK	128	eDP1_HPD# / LVDS_BLC_CLK	NC	AQ7-APL no support eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX	NC	AQ7-APL no support CAN0_TX	130	CAN0_RX	NC	AQ7-APL no support CAN0_RX

Connector Pinout Description

Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark	Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark
129	CAN0_TX	NC	AQ7-APL no support CAN0_TX	130	CAN0_RX	NC	AQ7-APL no support CAN0_RX
131	DP_LANE3+ / TMDS_CLK+	DP_LANE3+ / (TMDS_CLK+)	Option function is Gray font	132	USB_SSTX1-	USB_SSTX1-	
133	DP_LANE3- / TMDS_CLK-	DP_LANE3- / (TMDS_CLK-)	Option function is Gray font	134	USB_SSTX1+	USB_SSTX1+	
135	GND	GND		136	GND	GND	
137	DP_LANE1+ / TMDS_LANE1+	DP_LANE1+ / (TMDS_LANE1+)	Option function is Gray font	138	DP_AUX+	DP_AUX+	
139	DP_LANE1- / TMDS_LANE1-	DP_LANE1- / (TMDS_LANE1-)	Option function is Gray font	140	DP_AUX-	DP_AUX-	
141	GND	GND		142	GND	GND	
143	DP_LANE2+ / TMDS_LANE0+	DP_LANE2+ / (TMDS_LANE0+)	Option function is Gray font	144	USB_SSRX1-	USB_SSRX1-	
145	DP_LANE2- / TMDS_LANE0-	DP_LANE2- / (TMDS_LANE0-)	Option function is Gray font	146	USB_SSRX1+	USB_SSRX1+	
147	GND	GND		148	GND	GND	
149	DP_LANE0+ / TMDS_LANE2+	DP_LANE0+ / (TMDS_LANE2+)	Option function is Gray font	150	HDMI_CTRL_DAT	HDMI_CTRL_DAT	
151	DP_LANE0- / TMDS_LANE2-	DP_LANE0- / (TMDS_LANE2-)	Option function is Gray font	152	HDMI_CTRL_CLK	HDMI_CTRL_CLK	
153	HDMI_HPD#	HDMI_HPD#		154	DP_HPD#	DP_HPD#	
155	PCIE_CLK_REF+	PCIE_CLK_REF+		156	PCIE_WAKE#	PCIE_WAKE#	
157	PCIE_CLK_REF-	PCIE_CLK_REF-		158	PCIE_RST#	PCIE_RST#	
159	GND	GND		160	GND	GND	
161	PCIE3_TX+	PCIE3_TX+		162	PCIE3_RX+	PCIE3_RX+	
163	PCIE3_TX-	PCIE3_TX-		164	PCIE3_RX-	PCIE3_RX-	
165	GND	GND		166	GND	GND	
167	PCIE2_TX+	PCIE2_TX+		168	PCIE2_RX+	PCIE2_RX+	
169	PCIE2_TX-	PCIE2_TX-		170	PCIE2_RX-	PCIE2_RX-	
171	UART0_TX	UART0_TX		172	UART0_RTS#	UART0_RTS#	
173	PCIE1_TX+	PCIE1_TX+		174	PCIE1_RX+	PCIE1_RX+	
175	PCIE1_TX-	PCIE1_TX-		176	PCIE1_RX-	PCIE1_RX-	
177	UART0_RX	UART0_RX		178	UART0_CTS#	UART0_CTS#	
179	PCIE0_TX+	PCIE0_TX+		180	PCIE0_RX+	PCIE0_RX+	
181	PCIE0_TX-	PCIE0_TX-		182	PCIE0_RX-	PCIE0_RX-	
183	GND	GND		184	GND	GND	
185	LPC_AD0 / GPIO0	LPC_AD0 / (GPIO0)	Option function is Gray font	186	LPC_AD1 / GPIO1	LPC_AD1 / (GPIO1)	Option function is Gray font
187	LPC_AD2 / GPIO2	LPC_AD2 / (GPIO2)	Option function is Gray font	188	LPC_AD3 / GPIO3	LPC_AD3 / (GPIO3)	Option function is Gray font
189	LPC_CLK / GPIO4	LPC_CLK / (GPIO4)	Option function is Gray font	190	LPC_FRAME# / GPIO5	LPC_FRAME# / (GPIO5)	Option function is Gray font
191	SERIRQ / GPIO6	SERIRQ / (GPIO6)	Option function is Gray font	192	LPC_LDRQ# / GPIO7	(GPIO7)	AQ7-APL no support LPC_LDRQ# Remark : Option function is Gray font
193	VCC_RTC	VCC_RTC		194	SPKR / GP_PWM_OUT2	SPKR	AQ7-APL no support GP_PWM_OUT2

Connector Pinout Description

Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark	Pin	Signal for Qseven R21 SPEC	Signal for AQ7-APL A01 Design	Remark
193	VCC_RTC	VCC_RTC		194	SPKR / GP_PWM_OUT2	SPKR	AQ7-APL no support GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	FAN_TACHOIN	AQ7-APL no support GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1	FAN_PWMOUT	AQ7-APL no support GP_PWM_OUT1
197	GND	GND		198	GND	GND	
199	SPI_MOSI	SPI_MOSI		200	SPI_CS0#	SPI_CS0#	
201	SPI_MISO	SPI_MISO		202	SPI_CS1#	NC	
203	SPI_SCK	SPI_SCK		204	MFG_NC4	NC	
205	VCC_5V_SB	VCC_5V_SB		206	VCC_5V_SB	VCC_5V_SB	
207	MFG_NC0	NC	AQ7-APL no support MFG_NC0	208	MFG_NC2	NC	AQ7-APL no support MFG_NC2
209	MFG_NC1	NC	AQ7-APL no support MFG_NC1	210	MFG_NC3	NC	AQ7-APL no support MFG_NC3
211	NC*	NC		212	NC*	NC	
213	NC*	NC		214	NC*	NC	
215	NC*	NC		216	NC*	NC	
217	NC*	NC		218	NC*	NC	
219	VCC	VCC		220	VCC	VCC	
221	VCC	VCC		222	VCC	VCC	
223	VCC	VCC		224	VCC	VCC	
225	VCC	VCC		226	VCC	VCC	
227	VCC	VCC		228	VCC	VCC	
229	VCC	VCC		230	VCC	VCC	

Appendix II: AQ7-BT Module Pin Out (Qseven 2.0)

Connector Pinout Description

Pin	Signal for Qseven R20 SPEC	Signal for AQ7-BT A20 Design	Remark	Pin	Signal for Qseven R20 SPEC	Signal for AQ7-BT A20 Design	Remark
1	GND	GND21		2	GND	GND34	
3	GBE_MDI3-	LAN1_MDI3N		4	GBE_MDI2-	LAN1_MDI2N	
5	GBE_MDI3+	LAN1_MDI3P		6	GBE_MDI2+	LAN1_MDI2P	
7	GBE_LINK100#	LAN1_LED_100#		8	GBE_LINK1000#	LAN1_LED_1000#	
9	GBE_MDI1-	LAN1_MDI1N		10	GBE_MDI0-	LAN1_MDI0N	
11	GBE_MDI1+	LAN1_MDI1P		12	GBE_MDI0+	LAN1_MDI0P	
13	GBE_LINK#	LAN1_LED_LNK#_ACT		14	GBE_ACT#	LAN1_LED_LNK#_ACT	
15	GBE_CTREF	NC		16	SUS_S5#	O_SLP_S4	
17	WAKE#	I_Wake1#		18	SUS_S3#	O_SLP_S3	
19	SUS_STAT#	no connect	AQ7-BT no support SUS_STAT#	20	PWRBTN#	I_PS_IN#	
21	SLP_BTN#	CB_SLEEP#_V3.3A		22	LID_BTN#	CB_LID#_V3.3A	
23	GND	GND22		24	GND	GND33	
25	GND	GND23		26	PWGIN	I_PWRGD_CB	
27	BATLOW#	I_BATLOW#		28	RSTBTN#	CARRY_SYSRST#	
29	SATA0_TX+	SATA_TXP0		30	SATA1_TX+	NC	AQ7-BT no support SATA1_TX+
31	SATA0_TX-	SATA_TXN0		32	SATA1_TX-	NC	AQ7-BT no support SATA1_TX-
33	SATA_ACT#	SATA_LED_CB#		34	GND	GND32	
35	SATA0_RX+	SATA_RXP0		36	SATA1_RX+	NC	AQ7-BT no support SATA1_RX+
37	SATA0_RX-	SATA_RXN0		38	SATA1_RX-	NC	AQ7-BT no support SATA1_RX-
39	GND	GND24		40	GND	GND31	
41	BIOS_DISABLE#/BOOT_ALT#	BIOS_DISABLE#	AQ7-BT no support BOOT_ALT#	42	SDIO_CLK#	SDMMC3_CLK	
43	SDIO_CD#	SDMMC3_CD#		44	SDIO_LED	NC	AQ7-BT no support SDIO_LED
45	SDIO_CMD	SDMMC3_CMD		46	SDIO_WP	SDMMC3_WP	
47	SDIO_PWR#	NC	AQ7-BT no support SDIO_PWR#	48	SDIO_DAT1	SDMMC3_D1	
49	SDIO_DAT0	SDMMC3_D0		50	SDIO_DAT3	SDMMC3_D3	
51	SDIO_DAT2	SDMMC3_D2		52	SDIO_DAT5	NC	AQ7-BT no support SDIO_DAT5
53	SDIO_DAT4	NC	AQ7-BT no support SDIO_DAT4	54	SDIO_DAT7	NC	AQ7-BT no support SDIO_DAT7
55	SDIO_DAT6	NC	AQ7-BT no support SDIO_DAT6	56	RSVD	NC	NC
57	GND	GND25		58	GND	GND30	
59	HDA_SYNC/I2S_WS	CB_HDA_SYNC	AQ7-BT no support I2S_WS	60	SMB_CLK/GPI1_I2C_CLK	SMB_CLK_3.3S	AQ7-BT no support GP1_I2C_CLK
61	HDA_RST#/I2S_RST#	CB_HDA_RST#	AQ7-BT no support I2S_RST#	62	SMB_DAT/GPI1_I2C_DAT	SMB_DATA_3.3S	AQ7-BT no support GP1_I2C_DAT
63	HDA_BITCLK/I2C_CLK	CB_HDA_CLK	AQ7-BT no support I2S_CLK	64	SMB_ALERT#	SMB_ALERT#_3.3S	
65	HDA_SDI/I2S_SDI	CB_HDA_SDI0	AQ7-BT no support I2S_SDI	66	GP0_I2C_CLK	EC_CLK	
67	HDA_SDO/I2S_SDO	CB_HDA_SDO	AQ7-BT no support I2S_SDO	68	GP0_I2C_DAT	EC_DATA	
69	THRM#	NC	AQ7-BT no support THRM#	70	WDTRIG#	NC	AQ7-BT no support WDTRIG#
71	THRMTRIP#	I_THRMTRIP#		72	WDOUT	O_WDT#	
73	GND	GND26		74	GND	GND29	
75	USB_P7-/USB_SSTX0-	USB_SSTX0-	AQ7-BT no support USB_P7-	76	USB_P6-/USB_SSRX0-	USB_SSRX0-	AQ7-BT no support USB_P6-
77	USB_P7+/USB_SSTX0+	USB_SSTX0+	AQ7-BT no support USB_P7+	78	USB_P6+/USB_SSRX0+	USB_SSRX0+	AQ7-BT no support USB_P6+
79	USB_6_7_OC#	no connect		80	USB_4_5_OC#	USB_OC#_4_5	
81	USB_P5-/USB_SSTX1-	USB_DN5_CB	AQ7-BT no support USB_SSTX1-	82	USB_P4-/USB_SSRX1-	USB_DN4_CB	AQ7-BT no support USB_SSRX1-
83	USB_P5+/USB_SSTX1+	USB_DP5_CB	AQ7-BT no support USB_SSTX1+	84	USB_P4+/USB_SSRX1+	USB_DP4_CB	AQ7-BT no support USB_SSRX1+
85	USB_2_3_OC#	USB_OC#_2_3_3.3S		86	USB_0_1_OC#	USB_OC#_0_1_3.3S	
87	USB_P3-	USB_DN3_CB		88	USB_P2-	USB_DN2_CB	
89	USB_P3+	USB_DP3_CB		90	USB_P2+	USB_DP2_CB	
91	USB_CC	NC	AQ7-BT no support USB_CC	92	USB_ID	NC	AQ7-BT no support USB_ID
93	USB_P1-	USB_DN1_CB		94	USB_P0-	USB_DN0_CB	
95	USB_P1+	USB_DP1_CB		96	USB_P0+	USB_DP0_CB	
97	GND	GND27		98	GND	GND28	
99	eDP0_TX0+/LVDS_A0+	LVDS_A0+	AQ7-BT no support eDP0_TX0+	100	eDP1_TX0+/LVDS_B0+	NC	AQ7-BT no support eDP1_TX0+
101	eDP0_TX0-/LVDS_A0-	LVDS_A0-	AQ7-BT no support eDP0_TX0-	102	eDP1_TX0-/LVDS_B0-	NC	AQ7-BT no support eDP1_TX0-
103	eDP0_TX1+/LVDS_A1+	LVDS_A1+	AQ7-BT no support eDP0_TX1+	104	eDP1_TX1+/LVDS_B1+	NC	AQ7-BT no support eDP1_TX1+
105	eDP0_A1-/LVDS_A1-	LVDS_A1-	AQ7-BT no support eDP0_TX1-	106	eDP1_TX1-/LVDS_B1-	NC	AQ7-BT no support eDP1_TX1-
107	eDP0_TX2+/LVDS_A2+	LVDS_A2+	AQ7-BT no support eDP0_TX2+	108	eDP_TX2+/LVDS_B2+	NC	AQ7-BT no support eDP1_TX2+
109	eDP0_TX2-/LVDS_A2-	LVDS_A2-	AQ7-BT no support eDP0_TX2-	110	eDP_TX2-/LVDS_B2-	NC	AQ7-BT no support eDP1_TX2-
111	LVDS_PPEN	LVDS_VDD_EN		112	LVDS_BLEN	LVDS_BKLTEN	
113	eDP0_TX3+/LVDS_A3+	LVDS_A3+	AQ7-BT no support eDP0_TX3+	114	eDP_TX3+/LVDS_B3+	NC	AQ7-BT no support eDP1_TX3+
115	eDP0_TX3-/LVDS_A3-	LVDS_A3-	AQ7-BT no support eDP0_TX3-	116	eDP_TX3-/LVDS_B3-	NC	AQ7-BT no support eDP1_TX3-
117	GND	GND1		118	GND	GND9	
119	eDP0_AUX+/LVDS_A_CLK+	LVDS_A_CLK+	AQ7-BT no support eDP0_AUX+	120	eDP_AUX+/LVDS_B_CLK+	NC	AQ7-BT no support eDP1_AUX+
121	eDP0_AUX-/LVDS_A_CLK-	LVDS_A_CLK-	AQ7-BT no support eDP0_AUX-	122	eDP_AUX-/LVDS_B_CLK-	NC	AQ7-BT no support eDP1_AUX-
123	LVDS_BLT_CTRL/GP_PWM_OUT0	LVDS_BLT_CTRL	AQ7-BT no support GP_PWM_OUT0	124	GP_1-Wire_Bus	NC	AQ7-BT no support GP_1-Wire_Bus
125	GP2_I2C_DAT/LVDS_DID_DAT	LVDS_DID_DAT	AQ7-BT no support GP2_I2C_DAT	126	eDP0_HPD#/LVDS_BLC_DAT	NC	AQ7-BT no support LVDS_BLC_DAT
127	GP2_I2C_CLK/LVDS_DID_CLK	LVDS_DID_CLK	AQ7-BT no support GP2_I2C_CLK	128	eDP1_HPD#/LVDS_BLC_CLK	NC	AQ7-BT no support eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX	NC	AQ7-BT no support CAN0_TX	130	CAN0_RX	NC	AQ7-BT no support CAN0_RX
131	DP_LANE3+/TMDS_CLK+	HDMI_DP_PAIR3_P	Option function is Gray font	132	RSVD (Diff pair)	NC	NC
133	DP_LANE3-/TMDS_CLK-	HDMI_DP_PAIR3_N	Option function is Gray font	134	RSVD (Diff pair)	NC	NC
135	GND	GND2		136	GND	GND10	
137	DP_LANE1+/TMDS_LANE1+	HDMI_DP_PAIR1_P	Option function is Gray font	138	DP_AUX+	DDI0_DP_AUXP	
139	DP_LANE1-/TMDS_LANE1-	HDMI_DP_PAIR1_N	Option function is Gray font	140	DP_AUX-	DDI0_DP_AUXN	
141	GND	GND3		142	GND	GND11	

Connector Pinout Description

Pin	Signal for Qseven R20 SPEC	Signal for AQ7-BT A20 Design	Remark	Pin	Signal for Qseven R20 SPEC	Signal for AQ7-BT A20 Design	Remark
143	DP_LANE2+/TMDS_LANE0+	HDMI_DP_PAIR2_P	Option function is Gray font	144	RSVD (Diff pair)	NC	NC
145	DP_LANE2-/TMDS_LANE0-	HDMI_DP_PAIR2_N	Option function is Gray font	146	RSVD (Diff pair)	NC	NC
147	GND	GND4		148	GND	GND12	
149	DP_LANE0+/TMDS_LANE2+	HDMI_DP_PAIR0_P	Option function is Gray font	150	HDMI_CTRL_DAT	HDMI_DATA	
151	DP_LANE0-/TMDS_LANE2-	HDMI_DP_PAIR0_N	Option function is Gray font	152	HDMI_CTRL_CLK	HDMI_CLK	
153	DP_HDMI_HPD#	HDMI_DP_HPD		154	RSVD	HDMI_DP_HPD	
155	PCIE_CLK_REF+	CLK_PCIE_1_P		156	PCIE_WAKE#	I_Wake0#	
157	PCIE_CLK_REF-	CLK_PCIE_1_N		158	PCIE_RST#	I_LPCRST#	
159	GND	GND5		160	GND	GND13	
161	PCIE3_TX+	NC	AQ7-BT no support PCIE3_TX+	162	PCIE3_RX+	NC	AQ7-BT no support PCIE3_RX+
163	PCIE3_TX-	NC	AQ7-BT no support PCIE3_TX-	164	PCIE3_RX-	NC	AQ7-BT no support PCIE3_RX-
165	GND	GND6		166	GND	GND14	
167	PCIE2_TX+	PCIE_TXP2		168	PCIE2_RX+	PCIE_RXP2	
169	PCIE2_TX-	PCIE_TXN2		170	PCIE2_RX-	PCIE_RXN2	
171	UART0_TX	TXD		172	UART0_RTS#	UART0_RTS#	
173	PCIE1_TX+	PCIE_TXP1		174	PCIE1_RX+	PCIE_RXP1	
175	PCIE1_TX-	PCIE_TXN1		176	PCIE1_RX-	PCIE_RXN1	
177	UART0_RX	RXD		178	UART0_CTS#	UART0_CTS#	
179	PCIE0_TX+	PCIE_TXP0		180	PCIE0_RX+	PCIE_RXP0	
181	PCIE0_TX-	PCIE_TXN0		182	PCIE0_RX-	PCIE_RXN0	
183	GND	GND7		184	GND	GND15	
185	LPC_AD0/GPIO0	LPC_GPIO_AD0	Option function is Gray font	186	LPC_AD1/GPIO1	LPC_GPIO_AD1	Option function is Gray font
187	LPC_AD2/GPIO2	LPC_GPIO_AD2	Option function is Gray font	188	LPC_AD3/GPIO3	LPC_GPIO_AD3	Option function is Gray font
189	LPC_CLK/GPIO4	CLK_LPC_GPIO_CON	Option function is Gray font	190	LPC_FRAME#/GPIO5	LPC_GPIO_FRAME#	Option function is Gray font
191	SERIRQ/GPIO6	INT_GPIO_SERIRQ	Option function is Gray font	192	LPC_LDRQ#/GPIO7	GPIO7	AQ7-BT no support LPC_LDRQ# Remark : Option function is Gray font
193	VCC_RTC	CB_VRTC		194	SPKR/GP_PWM_OUT2	SPKR	AQ7-BT no support GP_PWM_OUT2
195	FAN_TACHOIN/GP_TIMER_IN	FAN_TACHOIN	AQ7-BT no support GP_TIMER_IN	196	FAN_PWMOUT/GP_PWM_OUT1	CB_FAN_PWM	AQ7-BT no support GP_PWM_OUT1
197	GND	GND8		198	GND	GND16	
199	SPI_MOSI	SPI_SI_F		200	SPI_CS0#	SPI_CS0#_F	
201	SPI_MISO	SPI_SO_F		202	SPI_CS1#	NC	AQ7-BT no support SPI_CS1#
203	SPI_CLK	SPI_CLK_F		204	MFG_NC4	NC	AQ7-BT no support MFG_NC4
205	VCC_5V_SB	VCC_5V_SBY		206	VCC_5V_SB	VCC_5V_SBY	
207	MFG_NC0	NC	AQ7-BT no support MFG_NC0	208	MFG_NC2	NC	AQ7-BT no support MFG_NC2
209	MFG_NC1	NC	AQ7-BT no support MFG_NC1	210	MFG_NC3	NC	AQ7-BT no support MFG_NC3
211	VCC	V5_MOD_IN		212	VCC	V5_MOD_IN	
213	VCC	V5_MOD_IN		214	VCC	V5_MOD_IN	
215	VCC	V5_MOD_IN		216	VCC	V5_MOD_IN	
217	VCC	V5_MOD_IN		218	VCC	V5_MOD_IN	
219	VCC	V5_MOD_IN		220	VCC	V5_MOD_IN	
221	VCC	V5_MOD_IN		222	VCC	V5_MOD_IN	
223	VCC	V5_MOD_IN		224	VCC	V5_MOD_IN	
225	VCC	V5_MOD_IN		226	VCC	V5_MOD_IN	
227	VCC	V5_MOD_IN		228	VCC	V5_MOD_IN	
229	VCC	V5_MOD_IN		230	VCC	V5_MOD_IN	

Appendix III: Qseven R2.1 versus AAEON ECB-970-A10

Based on Qseven 2.1 spec, the chart below listed the differences of R2.1 and the R2.0 carrier board ECB-970-A1.0 (Q7 R2.0). Additional remarks also added to describe AAEON's plan to update to ECB-970-A1.1 which follows R2.1 pin out.

Connector Pinout Description

Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark	Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark
1	GND	GND	GND	2	GND	GND	GND
3	GBE_MDI3-	GBE_MDI3-		4	GBE_MDI2-	GBE_MDI2-	
5	GBE_MDI3+	GBE_MDI3+		6	GBE_MDI2+	GBE_MDI2+	
7	GBE_LINK100#	GBE_LINK100#		8	GBE_LINK1000#	GBE_LINK1000#	
9	GBE_MDI1-	GBE_MDI1-		10	GBE_MDI0-	GBE_MDI0-	
11	GBE_MDI1+	GBE_MDI1+		12	GBE_MDI0+	GBE_MDI0+	
13	GBE_LINK#	GBE_LINK#		14	GBE_ACT#	GBE_ACT#	
15	GBE_CTREF	GBE_CTREF		16	SUS_S5#	SUS_S5#	
17	WAKE#	WAKE#		18	SUS_S3#	SUS_S3#	
19	GPO0	SUS_STAT#	change to GPO0 (Reserved :SUS_STAT#)	20	PWRBTN#	PWRBTN#	
21	SLP_BTN# / GPII1	SLEEP#	added resistor select for SLP_BTN# / GPII1	22	LID_BTN# / GPII0	LID#	added resistor select for SLP_BTN#
23	GND	GND	GND	24	GND	GND	GND
25	GND	GND	GND	26	PWGIN	PWR_OK	
27	BATLOW# / GPII2	BATLOW#	added resistor select for BATLOW# / GPII2	28	RSTBTN#	SYS_RESET#	
29	SATA0_TX+	SATA0_TX+		30	SATA1_TX+	SATA1_TX+	
31	SATA0_TX-	SATA0_TX-		32	SATA1_TX-	SATA1_TX-	
33	SATA_ACT#	SATA_LED#		34	GND	GND	GND
35	SATA0_RX+	SATA0_RX+		36	SATA1_RX+	SATA1_RX+	
37	SATA0_RX-	SATA0_RX-		38	SATA1_RX-	SATA1_RX-	
39	GND	GND		40	GND	GND	GND
41	BIOS_DISABLE# / BOOT_ALT#	BIOS_DISABLE#	added BOOT_ALT# share BIOS_DISABLE# pin	42	SDIO_CLK#	SDIO_CLK#	
43	SDIO_CD#	SDIO_CD#		44	reserved	SDIO_LED	Reserved
45	SDIO_CMD	SDIO_CMD		46	SDIO_WP	SDIO_WP	
47	SDIO_PWR#	SDIO_PWR#		48	SDIO_DAT1	SDIO_DAT1	
49	SDIO_DAT0	SDIO_DAT0		50	SDIO_DAT3	SDIO_DAT3	
51	SDIO_DAT2	SDIO_DAT2		52	reserved	SDIO_DAT5	NC (Reserved:SDIO_DATA5)
53	reserved	SDIO_DAT4	NC (Reserved:SDIO_DATA4)	54	reserved	SDIO_DAT7	NC (Reserved:SDIO_DATA7)
55	reserved	SDIO_DAT6	NC (Reserved:SDIO_DATA6)	56	USB_OTG_PEN	NC	
57	GND	GND		58	GND	GND	GND
59	HDA_SYNC / I2S_WS	AUDIO_SYNC	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	60	SMB_CLK / GP1_I2C_CLK	SMBCLK_SBY	SMBCLK_SBY

Connector Pinout Description

Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark	Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark
59	HDA_SYNC / I2S_WS	AUDIO_SYNC	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	60	SMB_CLK / GP1_I2C_CLK	SMBCLK_SBY	SMBCLK_SBY
61	HDA_RST# / I2S_RST#	AUDIO_RST#	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	62	SMB_DAT / GP1_I2C_DAT	SMBDAT_SBY	SMBDAT_SBY
63	HDA_BITCLK / I2S_CLK	AUDIO_BITCLK	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	64	SMB_ALERT#	SMB_ALERT#	
65	HDA_SDI / I2S_SDI	AUDIO_SDIN0	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	66	GP0_I2C_CLK	I2C_CK	
67	HDA_SDO / I2S_SDO	AUDIO_SDOUT	keep ECB-970 A10 HAD/I2S circuit (Jumper select)	68	GP0_I2C_DAT	I2C_DAT	
69	THRM#	THRM#		70	WDTRIG#	WDTRIG#	
71	THRMTRIP#	THRMTRIP#		72	WDOUT	WDT	
73	GND	GND		74	GND	GND	GND
75	USB_P7- / USB_SSTX0-	USB_P7-		76	USB_P6- / USB_SSRX0-	USB_P6-	
77	USB_P7+ / USB_SSTX0+	USB_P7+		78	USB_P6+ / USB_SSRX0+	USB_P6+	
79	USB_6_7_OC#	USB_6_7_OC#		80	USB_4_5_OC#	USB_4_5_OC#	
81	USB_P5- / USB_SSTX2-	USB_P5-	add switch IC (USB_P5- / USB_SSTX2-)	82	USB_P4- / USB_SSRX2-	USB_P4-	add switch IC (USB_P4- /
83	USB_P5+ / USB_SSTX2+	USB_P5+	add switch IC (USB_P5+ / USB_SSTX2+)	84	USB_P4+ / USB_SSRX2+	USB_P4+	add switch IC (USB_P4+ /
85	USB_2_3_OC#	USB_2_3_OC#		86	USB_0_1_OC#	USB_0_1_OC#	
87	USB_P3-	USB_P3-		88	USB_P2-	USB_P2-	
89	USB_P3+	USB_P3+		90	USB_P2+	USB_P2+	
91	USB_VBUS	USB_CC		92	USB_ID	USB_ID	
93	USB_P1-	USB_P1-		94	USB_P0-	USB_P0-	
95	USB_P1+	USB_P1+		96	USB_P0+	USB_P0+	
97	GND	GND		98	GND	GND	GND
99	eDP0_TX0+ / LVDS_A0+	LV_eDP_A0+		100	eDP1_TX0+ / LVDS_B0+	LV_eDP_B0+	LVDS default at ECB-970-A10 CN31
101	eDP0_TX0- / LVDS_A0-	LV_eDP_A0-		102	eDP1_TX0- / LVDS_B0-	LV_eDP_B0-	LVDS default at ECB-970-A10 CN31
103	eDP0_TX1+ / LVDS_A1+	LV_eDP_A1+		104	eDP1_TX1+ / LVDS_B1+	LV_eDP_B1+	LVDS default at ECB-970-A10 CN31
105	eDP0_TX1- / LVDS_A1-	LV_eDP_A1-		106	eDP1_TX1- / LVDS_B1-	LV_eDP_B1-	LVDS default at ECB-970-A10 CN31
107	eDP0_TX2+ / LVDS_A2+	LV_eDP_A2+		108	eDP1_TX2+ / LVDS_B2+	LV_eDP_B2+	LVDS default at ECB-970-A10 CN31
109	eDP0_TX2- / LVDS_A2-	LV_eDP_A2-		110	eDP1_TX2- / LVDS_B2-	LV_eDP_B2-	LVDS default at ECB-970-A10 CN31
111	LVDS_PPEN	LVDS_VDD_EN		112	LVDS_BLEN	LVDS_BKLT_EN	
113	eDP0_TX3+ / LVDS_A3+	LV_eDP_A3+		114	eDP1_TX3+ / LVDS_B3+	LV_eDP_B3+	LVDS default at ECB-970-A10 CN31

Connector Pinout Description							
Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark	Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark
115	eDP0_TX3- / LVDS_A3-	LV_eDP_A3-		116	eDP1_TX3- / LVDS_B3-	LV_eDP_B3-	LVDS default at ECB-970-A10 CN31
117	GND	GND		118	GND	GND	GND
119	eDP0_AUX+ / LVDS_A_CLK+	LV_eDP_A_CK+		120	eDP1_AUX+ / LVDS_B_CLK+	LV_eDP_B_CK+	LVDS default at ECB-970-A10 CN31
121	eDP0_AUX- / LVDS_A_CLK-	LV_eDP_A_CK-		122	eDP1_AUX- / LVDS_B_CLK-	LV_eDP_B_CK-	LVDS default at ECB-970-A10 CN31
123	LVDS_BLT_CTRL / GP_PWM_OUT0	LV_eDP_BKLT_CTRL		124	GP_1-Wire_Bus / HDMI_CEC	NC	CEC Design TBD
125	GP2_I2C_DAT / LVDS_DID_DAT	LV_eDP_DDCDAT		126	eDP0_HPD# / LVDS_BLC_DAT	LV_eDP_BLC_DDCDAT	
127	GP2_I2C_CLK / LVDS_DID_CLK	LV_eDP_DDCCLK		128	eDP1_HPD# / LVDS_BLC_CLK	LV_eDP_BLC_DDCCLK	
129	CAN0_TX	CAN_TX		130	CAN0_RX	CAN_RX	
131	DP_LANE3+ / TMDS_CLK+	HDMI_DP_PAIR3+		132	USB_SSTX1-	NC	add USB3.0 connector & Repeater
133	DP_LANE3- / TMDS_CLK-	HDMI_DP_PAIR3-		134	USB_SSTX1+	NC	add USB3.0 connector & Repeater
135	GND			136	GND	GND	GND
137	DP_LANE1+ / TMDS_LANE1+	HDMI_DP_PAIR1+		138	DP_AUX+	DP_CTRLCLK_AUX+	
139	DP_LANE1- / TMDS_LANE1-	HDMI_DP_PAIR1-		140	DP_AUX-	DP_CTRLDATA_AUX-	
141	GND			142	GND	GND	GND
143	DP_LANE2+ / TMDS_LANE0+	HDMI_DP_PAIR2+		144	USB_SSRX1-	NC	add USB3.0 connector & Repeater
145	DP_LANE2- / TMDS_LANE0-	HDMI_DP_PAIR2		146	USB_SSRX1+	NC	add USB3.0 connector & Repeater
147	GND	GND		148	GND	GND	GND
149	DP_LANE0+ / TMDS_LANE2+	HDMI_DP_PAIR0+		150	HDMI_CTRL_DAT	HDMI_CTRL_DAT	
151	DP_LANE0- / TMDS_LANE2-	HDMI_DP_PAIR0-		152	HDMI_CTRL_CLK	HDMI_CTRL_CLK	
153	HDMI_HPD#	HDMI_HPD#		154	DP_HPD#	DP_HPD	
155	PCIE_CLK_REF+	PCIE_CLK_REF+		156	PCIE_WAKE#	PCIE_WAKE#	
157	PCIE_CLK_REF-	PCIE_CLK_REF-		158	PCIE_RST#	PCIE_RST#	
159	GND	GND		160	GND	GND	GND
161	PCIE3_TX+	PCIE_TX3+		162	PCIE3_RX+	PCIE_RX3+	
163	PCIE3_TX-	PCIE_TX3-		164	PCIE3_RX-	PCIE_RX3-	
165	GND	GND		166	GND	GND	GND
167	PCIE2_TX+	PCIE_TX2+		168	PCIE2_RX+	PCIE_RX2+	
169	PCIE2_TX-	PCIE_TX2-		170	PCIE2_RX-	PCIE_RX2-	
171	UART0_TX	UART1_TXD		172	UART0_RTS#	UART1_RTSD	
173	PCIE1_TX+	PCIE_TX1+		174	PCIE1_RX+	PCIE_RX1+	

Connector Pinout Description							
Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark	Pin	Signal for Qseven R21	Signal for ECB-970 A1.0 (Qseven R20)	ECB-970-R21 Remark
175	PCIE1_TX-	PCIE_TX1-		176	PCIE1_RX-	PCIE_RX1-	
177	UART0_RX	UART1_RXD		178	UART0_CTS#	UART1_CTSD	
179	PCIE0_TX+	PCIE_TX0+		180	PCIE0_RX+	PCIE_RX0+	
181	PCIE0_TX-	PCIE_TX0-		182	PCIE0_RX-	PCIE_RX0-	
183	GND	GND		184	GND	GND	GND
185	LPC_AD0 / GPIO0	LPC_AD0	add switch for LPC_AD0 / GPIO0	186	LPC_AD1 / GPIO1	LPC_AD1	add switch for LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2	LPC_AD2	add switch for LPC_AD2 / GPIO2	188	LPC_AD3 / GPIO3	LPC_AD3	add switch for LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4	LPC_CLK		190	LPC_FRAME# / GPIO5	LPC_FRAME#	add switch for LPC_FRAME# /
191	SERIRQ / GPIO6	LPC_SERIRQ	add switch for SERIRQ / GPIO6	192	LPC_LDRQ# / GPIO7	LPC_DRQ0#	add switch for LPC_LDRQ# / GPIO7
193	VCC_RTC	RTCBAT		194	SPKR / GP_PWM_OUT2	SPKR	
195	FAN_TACHOIN / GP_TIMER_IN	FAN_TACHIN		196	FAN_PWMOUT / GP_PWM_OUT1	FAN_PWMOUT	
197	GND	GND		198	GND	GND	GND
199	SPI_MOSI	SPI_MOSI		200	SPI_CS0#	SPI_CS0#	
201	SPI_MISO	SPI_MISO		202	SPI_CS1#	NC	
203	SPI_SCK	SPI_CLK		204	MFG_NC4	MFG_NC4	
205	VCC_5V_SB	VCC_5V_SB		206	VCC_5V_SB	VCC_5V_SB	
207	MFG_NC0	TCK_M		208	MFG_NC2	TDO_M	
209	MFG_NC1	TMS_M		210	MFG_NC3	TDI_M	
211	NC*	VCC	NC (Reserved:VCC)	212	NC*	VCC	NC (Reserved:VCC)
213	NC*	VCC		214	NC*	VCC	
215	NC*	VCC		216	NC*	VCC	
217	NC*	VCC		218	NC*	VCC	
219	VCC	VCC	Confirm design for 5V & DC IN 19V/12V	220	VCC	VCC	Confirm design for 5V & DC IN 19V/12V
221	VCC	VCC		222	VCC	VCC	
223	VCC	VCC		224	VCC	VCC	
225	VCC	VCC		226	VCC	VCC	
227	VCC	VCC		228	VCC	VCC	
229	VCC	VCC		230	VCC	VCC	