Design Guide for
COM Express Type 6,7 & Type 10
Carrier Board

Edit by ECD Dept.

Version : 1.2
Date : 2020 / 03 / 16

Company Profile

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Committed to innovative engineering, AAEON provides integrated solutions, hardware and services for premier OEM/ODMs and system integrators worldwide. Reliable and high quality computing platforms include industrial motherboards and systems, industrial displays, rugged tablets, PC/104, PICMG and COM modules, embedded SBCs, embedded controllers, network appliances and related accessories. AAEON also offers customized end-to-end services from initial product conceptualization and product development on through to volume manufacturing and after-sales service programs.
With a continuous pursuit of innovation and excellence, AAEON became a member of the ASUS group in 2011, further strengthening its leadership fueled by advanced technology from ASUS and leveraging resources within the group. AAEON is posed to offer more diversified embedded products and solutions at higher quality standards to meet world-class design and manufacturing demands in the years to come.
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Reliability: Delivering trustworthy products on a timely manner to our customers
Integrity: We value business integrity and ethics, making AAEON your choice business partner
Innovation: Working abreast with industry leaders to maintain technology leadership, AAEON is able to help customers turn cutting-edge concepts into reality

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Revision History

Version	Release Date	Remark
V0.1	AUG 24, 2016	First release
V1.0	SEP 1, 2016	Publish
V1.1	JAN 21, 2019	Update eDP on page 49, DP on page 53, RTC on page 64, TYPE0#, TYPE1#, TYPE2# on page 71 and Rev 3.0 pin-out on page 11.
V1.2	Mar 6, 2020	Update Type 7 design guide

1. Introduction

1.1 Document Overview

Brief description of each chapter is given below :

Chapter 1: Introduction

Chapter 1 briefly introduces the pinout of type 6 &7& 10 and the structure of the design guide document.

Chapter 2: COM Express Mechanical Specification

Detailed information about the COM Express connector placement and dimensions are described in Chapter2.

Chapter 3: Signal Description and Routing Guideline

General design schemes and recommended layout rules are shown in chapter 3. This chapter contains board descriptions and general layout and routing guidelines for a COM Express Carrier Board. These design recommendations should be followed for a better quality and robustness.

Chapter 4: Power and Reset

Introduce ATX/AT power supplies and described the power sequence in detail.

1.2 Acronyms

1.2.1 Abbreviations and Definitions Used

Table 1-1: Abbreviations and Definitions Used

Term	Description
AC '97 / HDA	Audio CODEC '97/High Definition Audio
ACPI	Advanced Configuration Power Interface – standard to implement power saving modes in PCAT systems
BIOS	Basic Input Output System – firmware in PC-AT system that is used to initialize system components before handing control over to the operating system
BMC	Baseboard Management Controller
CAN	Controller-area network (CAN or CAN-bus) is a vehicle bus standard designed to allow microcontrollers to communicate with each other within a vehicle without a host computer.
Carrier Board	An application specific circuit board that accepts a COM Express Module.
DAC	Digital Analog Converter
DDC	Display Data Control – VESA (Video Electronics Standards Association) standard to allow identification of the capabilities of a VGA monitor
DDI	Digital Display Interface– containing DisplayPort, HDMI/DVI and SDVO
DP	DisplayPort is a digital display interface standard put forth by the Video Electronics Standards Association (VESA). It defines a new license free, royalty free, digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.
DVI	Digital Visual Interface - a Digital Display Working Group (DDWG) standard that defines a standard video interface supporting both digital and analog video signals. The digital signals use TMDS.
EDID	Extended Display Identification Data
eDP	Embedded DisplayPort (eDP) is a digital display interface standard produced by the Video Electronics Standards Association (VESA) for digital interconnect of Audio and Video.
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
Express Card	A PCMCIA standard built on the latest USB 2.0 and PCI Express

	buses
EAPI	Embedded Application Programming Interface Software interface for COM Express specific industrial functions • System information • Watchdog timer • I2C Bus • Flat Panel brightness control • User storage area • GPIO
eSPI	Enhanced Serial Peripheral Interface
GBE	Gigabit Ethernet
GPIO	General Purpose Input Output
HDMI	High Definition Multimedia Interface
I2C	Inter Integrated Circuit – 2 wire (clock and data) signaling scheme allowing communication between integrated circuits, primarily used to read and load register values.
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
LVDS	Low-Voltage Differential Signaling – widely used as a physical interface for TFT flat panels. LVDS can be used for many high-speed signaling applications. In this document, it refers only to TFT flat-panel applications.
MDIO	Management Data Input/Output, or MDIO, is a 2-wire serial bus that is used to manage PHYs or physical layer devices in media access controllers (MACs).
NC-SI	Network Controller Sideband Interface
PCI Express (PCIE)	Peripheral Component Interface Express – next-generation high speed Serialized I/O bus
PEG	PCI Express Graphics
RTC	Real Time Clock – battery backed circuit in PC-AT systems that keeps system time and date as well as certain system setup parameters
S0, S1, S2, S3, S4, S5	Sleep States defined by the ACPI specificationS0 Full power, all devices powered S1: Sleep State, all context maintained S2: Sleep State, CPU and Cache context lost S3: Suspend to RAM System context stored in RAM; RAM is in standby

	S4: Suspend to Disk System context stored on disk S5: Soft Off Main power rail off, only standby power rail present
SATA	Serial AT Attachment: serial-interface standard for hard disks
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SAFS	eSPI tTerm for Slave Attached Flash Sharing where the Flash component is attached behind a BMC component.
SGMII	Serial Gigabit Media Independent Interface
USB	Universal Serial Bus
WDT	Watch Dog Timer
TVS	Transient Voltage Suppressors
TPM	Trusted Platform Module, chip to enhance the security features of a computer system.
VDR (Varistor)	Voltage Dependent Resistor
10GBase-KR	10 Gbit internal copper interface. Operates over a single lane and uses the same physical layer coding (defined in IEEE 802.3 Clause 49) as 10GBASE-LR (Single Mode Fiber 1310 nm) /ER (Single Mode Fiber 1550 nm) /SR (Multi Mode Fiber 850 nm)
10GBase-KX4	4x 10 Gbit internal copper interface. Operates over four lanes and uses the same physical layer coding (defined in IEEE 802.3 Clause 48) as 10GBASE-CX4

1.2.2 Signal Table Terminology Descriptions

Table 1-2: Signal Table Terminology Descriptions

Term	Description
I/O 3.3V	Bi-directional signal 3.3V tolerant
I/O 5V	Bi-directional signal 5V tolerant
I 3.3V	Input 3.3V tolerant
I 5V	Input 5V tolerant
I/O 3V3_SBY	Bi-directional 3.3V tolerant active during Suspend and running state.
O 3.3V	Output 3.3V signal level
O 5V	Output 5V signal level
OD	Open drain output
P	Power input/output
PCIE	In compliance with PCI Express Base Specification
REF	Reference voltage output. May be sourced from a Module power plane.
PDS	Pull-down strap. A Module output pin that is either tied to GND or is not connected. Used to signal Module capabilities (pin-out type) to the Carrier Board.

1.3 COM Express Type 6 & Type 10 & Type 7 Pinout Comparison

Table 1-3: COM Express Type 6 & Type 10 Pinout (Refer PICMG Module DG Rev 3.0)

Pin	Type 6	Type 10	Type 7
A1	GND	GND	GND
A2	GBE0_MDI3-	GBE0_MDI3-	GBE0_MDI3-
A3	GBE0_MDI3+	GBE0_MDI3+	GBE0_MDI3+
A4	GBE0_LNIK100#	GBE0_LNIK100#	GBE0_LNIK100#
A5	GBE0_LNIK1000#	GBE0_LNIK1000#	GBE0_LNIK1000#
A6	GBE0_MDI2-	GBE0_MDI2-	GBE0_MDI2-
A7	GBE0_MDI2+	GBE0_MDI2+	GBE0_MDI2+
A8	GBE0_LINK#	GBE0_LINK#	GBE0_LINK#
A9	GBE0_MDI1-	GBE0_MDI1-	GBE0_MDI1-
A10	GBE0_MDI1+	GBE0_MDI1+	GBE0_MDI1+
A11	GND	GND	GND
A12	GBE0_MDI0-	GBE0_MDI0-	GBE0_MDI0-
A13	GBE0_MDI0+	GBE0_MDI0+	GBE0_MDI0+
A14	GBE0_CTREF	GBE0_CTREF	GBE0_CTREF
A15	SUS_S3#	SUS_S3#	SUS_S3#
A16	SATA0_TX+	SATA0_TX+	SATA0_TX+
A17	SATA0_TX-	SATA0_TX-	SATA0_TX-
A18	SUS_S4#	SUS_S4#	SUS_S4#
A19	SATA0_RX+	SATA0_RX+	SATA0_RX+
A20	SATA0_RX-	SATA0_RX-	SATA0_RX-
A21	GND	GND	GND
A22	SATA2_TX+	USB_SSRX0-	PCIE_TX15+
A23	SATA2_TX-	USB_SSRX0+	PCIE_TX15-
A24	SUS_S5#	SUS_S5#	SUS_S5#
A25	SATA2_RX+	USB_SSRX1-	PCIE_TX14+
A26	SATA2_RX-	USB_SSRX1+	PCIE_TX14-
A27	BATLOW#	BATLOW#	BATLOW#
A28	(S)ATA_ACT#	(S)ATA_ACT#	(S)ATA_ACT#
A29	AC/HDA_SYNC	AC/HDA_SYNC	RSVD
A30	AC/HDA_RST#	AC/HDA_RST#	RSVD
A31	GND	GND	GND
A32	AC/HDA_BITCLK	AC/HDA_BITCLK	RSVD
A33	AC/HDA_SDOUT	AC/HDA_SDOUT	RSVD
A34	BIOS_DIS0#/ESPI_SAFS	BIOS_DIS0#/ESPI_SAFS	BIOS_DIS0#/ESPI_SAFS
A35	THRMTRIP#	THRMTRIP#	THRMTRIP#
A36	USB6-	USB6-	PCIE_TX13+

Pin	Type 6	Type 10	Type 7
A37	USB6+	USB6+	PCIE_TX13-
A38	USB_6_7_OC#	USB_6_7_OC#	GND
A39	USB4-	USB4-	PCIE_TX12+
A40	USB4+	USB4+	PCIE_TX12-
A41	GND	GND	GND
A42	USB2-	USB2-	USB2-
A43	USB2+	USB2+	USB2+
A44	USB_2_3_OC#	USB_2_3_OC#	USB_2_3_OC#
A45	USB0-	USB0-	USB0-
A46	USB0+	USB0+	USB0+
A47	VCC_RTC	VCC_RTC	VCC_RTC
A48	RSVD	RSVD	RSVD
A49	GBE0_SDP	GBE0_SDP	GBE0_SDP
A50	LPC_SERIRQ/ESPI_CS1#	LPC_SERIRQ/ESPI_CS1#	LPC_SERIRQ/ESPI_CS1#
A51	GND	GND	GND
A52	PCIE_TX5+	RSVD	PCIE_TX5+
A53	PCIE_TX5-	RSVD	PCIE_TX5-
A54	GPI0	GPI0	GPI0
A55	PCIE_TX4+	RSVD	PCIE_TX4+
A56	PCIE_TX4-	RSVD	PCIE_TX4-
A57	GND	GND	GND
A58	PCIE_TX3+	PCIE_TX3+	PCIE_TX3+
A59	PCIE_TX3-	PCIE_TX3-	PCIE_TX3-
A60	GND	GND	GND
A61	PCIE_TX2+	PCIE_TX2+	PCIE_TX2+
A62	PCIE_TX2-	PCIE_TX2-	PCIE_TX2-
A63	GPI1	GPI1	GPI1
A64	PCIE_TX1+	PCIE_TX1+	PCIE_TX1+
A65	PCIE_TX1-	PCIE_TX1-	PCIE_TX1-
A66	GND	GND	GND
A67	GPI2	GPI2	GPI2
A68	PCIE_TX0+	PCIE_TX0+	PCIE_TX0+
A69	PCIE_TX0-	PCIE_TX0-	PCIE_TX0-
A70	GND	GND	GND
A71	LVDS_A0+	LVDS_A0+	PCIE_TX8+
A72	LVDS_A0-	LVDS_A0-	PCIE_TX8-
A73	LVDS_A1+	LVDS_A1+	GND

Pin	Type 6	Type 10	Type 7
A74	LVDS_A1-	LVDS_A1-	PCIE_TX9+
A75	LVDS_A2+	LVDS_A2+	PCIE_TX9-
A76	LVDS_A2-	LVDS_A2-	GND
A77	LVDS_VDD_EN	LVDS_VDD_EN	PCIE_TX10+
A78	LVDS_A3+	LVDS_A3+	PCIE_TX10-
A79	LVDS_A3-	LVDS_A3-	GND
A80	GND	GND	GND
A81	LVDS_A_CK+	LVDS_A_CK+	PCIE_TX11+
A82	LVDS_A_CK-	LVDS_A_CK-	PCIE_TX11-
A83	LVDS_I2C_CK	LVDS_I2C_CK	GND
A84	LVDS_I2C_DAT	LVDS_I2C_DAT	NCSI_TX_EN
A85	GPI3	GPI3	GPI3
A86	RSVD	RSVD	RSVD
A87	eDP_HPD	eDP_HPD	RSVD
A88	PCIE_CLK_REF+	PCIE_CLK_REF+	PCIE_CLK_REF+
A89	PCIE_CLK_REF-	PCIE_CLK_REF-	PCIE_CLK_REF-
A90	GND	GND	GND
A91	SPI_POWER	SPI_POWER	SPI_POWER
A92	SPI_MISO	SPI_MISO	SPI_MISO
A93	GPO0	GPO0	GPO0
A94	SPI_CLK	SPI_CLK	SPI_CLK
A95	SPI_MOSI	SPI_MOSI	SPI_MOSI
A96	TPM_PP	TPM_PP	TPM_PP
A97	TYPE10#	TYPE10#	TYPE10#
A98	SER0_TX	SER0_TX	SER0_TX
A99	SER0_RX	SER0_RX	SER0_RX
A100	GND	GND	GND
A101	SER1_TX	SER1_TX	SER1_TX
A102	SER1_RX	SER1_RX	SER1_RX
A103	LID#	LID#	LID#
A104	VCC_12V	VCC_12V	VCC_12V
A105	VCC_12V	VCC_12V	VCC_12V
A106	VCC_12V	VCC_12V	VCC_12V
A107	VCC_12V	VCC_12V	VCC_12V
A108	VCC_12V	VCC_12V	VCC_12V
A109	VCC_12V	VCC_12V	VCC_12V
A110	GND	GND	GND

Pin	Type 6	Type 10	Type 7
B1	GND	GND	GND
B2	GBE0_ACT#	GBE0_ACT#	GBE0_ACT#
B3	LPC_FRAME#/ESPI_CS0#	LPC_FRAME#/ESPI_CS0#	LPC_FRAME#/ESPI_CS0#
B4	LPC_AD0/ESPI_IO_0	LPC_AD0/ESPI_IO_0	LPC_AD0/ESPI_IO_0
B5	LPC_AD1/ESPI_IO_1	LPC_AD1/ESPI_IO_1	LPC_AD1/ESPI_IO_1
B6	LPC_AD2/ESPI_IO_2	LPC_AD2/ESPI_IO_2	LPC_AD2/ESPI_IO_2
B7	LPC_AD3/ESPI_IO_3	LPC_AD3/ESPI_IO_3	LPC_AD3/ESPI_IO_3
B8	LPC_DRQ0#/ESPI_ALERT0#	LPC_DRQ0#/ESPI_ALERT0#	LPC_DRQ0#/ESPI_ALERT0#
B9	LPC_DRQ1#/ESPI_ALERT1#	LPC_DRQ1#/ESPI_ALERT1#	LPC_DRQ1#/ESPI_ALERT1#
B10	LPC_CLK/ESPI_CK	LPC_CLK/ESPI_CK	LPC_CLK/ESPI_CK
B11	GND	GND	GND
B12	PWRBTN#	PWRBTN#	PWRBTN#
B13	SMB_CK	SMB_CK	SMB_CK
B14	SMB_DAT	SMB_DAT	SMB_DAT
B15	SMB_ALERT#	SMB_ALERT#	SMB_ALERT#
B16	SATA1_TX+	SATA1_TX+	SATA1_TX+
B17	SATA1_TX-	SATA1_TX-	SATA1_TX-
B18	SUS_STAT#/ESPI_RESET#	SUS_STAT#/ESPI_RESET#	SUS_STAT#/ESPI_RESET#
B19	SATA1_RX+	SATA1_RX+	SATA1_RX+
B20	SATA1_RX-	SATA1_RX-	SATA1_RX-
B21	GND	GND	GND
B22	SATA3_TX+	USB_SSTX0-	PCIE_RX15+
B23	SATA3_TX-	USB_SSTX0+	PCIE_RX15-
B24	PWR_OK	PWR_OK	PWR_OK
B25	SATA3_RX+	USB_SSTX1-	PCIE_RX14+
B26	SATA3_RX-	USB_SSTX1+	PCIE_RX14-
B27	WDT	WDT	WDT
B28	AC/HDA_SDIN2	AC/HDA_SDIN2	RSVD
B29	AC/HDA_SDIN1	AC/HDA_SDIN1	RSVD
B30	AC/HDA_SDIN0	AC/HDA_SDIN0	RSVD
B31	GND	GND	GND
B32	SPKR	SPKR	SPKR
B33	I2C_CK	I2C_CK	I2C_CK
B34	I2C_DAT	I2C_DAT	I2C_DAT
B35	THRM#	THRM#	THRM#
B36	USB7-	USB7-	PCIE_RX13+
B37	USB7+	USB7+	PCIE_RX13-

Pin	Type 6	Type 10	Type 7
B38	USB_4_5_OC#	USB_4_5_OC#	GND
B39	USB5-	USB5-	PCIE_RX12+
B40	USB5+	USB5+	PCIE_RX12-
B41	GND	GND	GND
B42	USB3-	USB3-	USB3-
B43	USB3+	USB3+	USB3+
B44	USB_0_1_OC#	USB_0_1_OC#	USB_0_1_OC#
B45	USB1-	USB1-	USB1-
B46	USB1+	USB1+	USB1+
B47	ESPI_EN#	ESPI_EN#	ESPI_EN#
B48	USB0_HOST_PRSNT	USB0_HOST_PRSNT	USB0_HOST_PRSNT
B49	SYS_RESET#	SYS_RESET#	SYS_RESET#
B50	CB_RESET#	CB_RESET#	CB_RESET#
B51	GND	GND	GND
B52	PCIE_RX5+	RSVD	PCIE_RX5+
B53	PCIE_RX5-	RSVD	PCIE_RX5-
B54	GPO1	GPO1	GPO1
B55	PCIE_RX4+	RSVD	PCIE_RX4+
B56	PCIE_RX4-	RSVD	PCIE_RX4-
B57	GPO2	GPO2	GPO2
B58	PCIE_RX3+	PCIE_RX3+	PCIE_RX3+
B59	PCIE_RX3-	PCIE_RX3-	PCIE_RX3-
B60	GND	GND	GND
B61	PCIE_RX2+	PCIE_RX2+	PCIE_RX2+
B62	PCIE_RX2-	PCIE_RX2-	PCIE_RX2-
B63	GPO3	GPO3	GPO3
B64	PCIE_RX1+	PCIE_RX1+	PCIE_RX1+
B65	PCIE_RX1-	PCIE_RX1-	PCIE_RX1-
B66	WAKE0#	WAKE0#	WAKE0#
B67	WAKE1#	WAKE1#	WAKE1#
B68	PCIE_RX0+	PCIE_RX0+	PCIE_RX0+
B69	PCIE_RX0-	PCIE_RX0-	PCIE_RX0-
B70	GND	GND	GND
B71	LVDS_B0+	DDI0_PAIR0+	PCIE_RX8+
B72	LVDS_B0-	DDI0_PAIR0-	PCIE_RX8-
B73	LVDS_B1+	DDI0_PAIR1+	GND
B74	LVDS_B1-	DDI0_PAIR1-	PCIE_RX9+

Pin	Type 6	Type 10	Type 7
B75	LVDS_B2+	DDI0_PAIR2+	PCIE_RX9-
B76	LVDS_B2-	DDI0_PAIR2-	GND
B77	LVDS_B3+	DDI0_PAIR4+	PCIE_RX10+
B78	LVDS_B3-	DDI0_PAIR4-	PCIE_RX10-
B79	LVDS_BKLT_EN	LVDS_BKLT_EN	GND
B80	GND	GND	GND
B81	LVDS_B_CK+	DDI0_PAIR3+	PCIE_RX11+
B82	LVDS_B_CK-	DDI0_PAIR3-	PCIE_RX11-
B83	LVDS_BKLT_CTRL	LVDS_BKLT_CTRL	GND
B84	VCC_5V_SBY	VCC_5V_SBY	VCC_5V_SBY
B85	VCC_5V_SBY	VCC_5V_SBY	VCC_5V_SBY
B86	VCC_5V_SBY	VCC_5V_SBY	VCC_5V_SBY
B87	VCC_5V_SBY	VCC_5V_SBY	VCC_5V_SBY
B88	BIOS_DIS1#	BIOS_DIS1#	BIOS_DIS1#
B89	VGA_RED	DDI0_HPD	NCSI_RX_ER
B90	GND	GND	GND
B91	VGA_GRN	DDI0_PAIR5+	NCSI_CLK_IN
B92	VGA_BLU	DDI0_PAIR5-	NCSI_RXD1
B93	VGA_HSYNC	DDI0_PAIR6+	NCSI_RXD0
B94	VGA_VSYNC	DDI0_PAIR6-	NCSI_CRS_DV
B95	VGA_I2C_CK	DDI0_DDC_AUX_SEL	NCSI_TXD1
B96	VGA_I2C_DAT	USB7_HOST_PRSNT	NCSI_TXD0
B97	SPI_CS#	SPI_CS#	SPI_CS#
B98	RSVD	DDI0_CTRLCLK_AUX+	NCSI_ARB_IN
B99	RSVD	DDI0_CTRLDATA_AUX-	NCSI_ARB_OUT
B100	GND	GND	GND
B101	FAN_PWMOUT	FAN_PWMOUT	FAN_PWMOUT
B102	FAN_TACHIN	FAN_TACHIN	FAN_TACHIN
B103	SLEEP#	SLEEP#	SLEEP#
B104	VCC_12V	VCC_12V	VCC_12V
B105	VCC_12V	VCC_12V	VCC_12V
B106	VCC_12V	VCC_12V	VCC_12V
B107	VCC_12V	VCC_12V	VCC_12V
B108	VCC_12V	VCC_12V	VCC_12V
B109	VCC_12V	VCC_12V	VCC_12V
B110	GND	GND	GND

Pin	Type 6	Type 7
C1	GND	GND
C2	GND	GND
C3	USB_SSRX0-	USB_SSRX0-
C4	USB_SSRX0+	USB_SSRX0+
C5	GND	GND
C6	USB_SSRX1-	USB_SSRX1-
C7	USB_SSRX1+	USB_SSRX1+
C8	GND	GND
C9	USB_SSRX2-	USB_SSRX2-
C10	USB_SSRX2+	USB_SSRX2+
C11	GND	GND
C12	USB_SSRX3-	USB_SSRX3-
C13	USB_SSRX3+	USB_SSRX3+
C14	GND	GND
C15	DDI1_PAIR6+	10G_PHY_MDC_SCL3
C16	DDI1_PAIR6-	10G_PHY_MDC_SCL2
C17	RSVD	10G_SDP2
C18	RSVD	GND
C19	PCIE_RX6+	PCIE_RX6+
C20	PCIE_RX6-	PCIE_RX6-
C21	GND	GND
C22	PCIE_RX7+	PCIE_RX7+
C23	PCIE_RX7-	PCIE_RX7-
C24	DDI1_HPD	10G_INT2
C25	DDI1_PAIR4+	GND
C26	DDI1_PAIR4-	10G_KR_RX3+
C27	RSVD	10G_KR_RX3-
C28	RSVD	GND
C29	DDI1_PAIR5+	10G_KR_RX2+
C30	DDI1_PAIR5-	10G_KR_RX2-
C31	GND	GND
C32	DDI2_CTRLCLK_AUX+	10G_SFP_SDA3
C33	DDI2_CTRLDATA_AUX-	10G_SFP_SDA2
C34	DDI2_DDC_AUX_SEL	10G_PHY_RST_23
C35	RSVD	10G_PHY_RST_01
C36	DDI3_CTRLCLK_AUX+	10G_LED_SDA
C37	DDI3_CTRLDATA_AUX-	10G_LED_SCL

Pin	Type 6	Type 7
C38	DDI3_DDC_AUX_SEL	10G_SFP_SDA1
C39	DDI3_PAIR0+	10G_SFP_SDA0
C40	DDI3_PAIR0-	10G_SDP0
C41	GND	GND
C42	DDI3_PAIR1+	10G_KR_RX1+
C43	DDI3_PAIR1-	10G_KR_RX1-
C44	DDI3_HPD	GND
C45	RSVD	10G_PHY_MDC_SCL1
C46	DDI3_PAIR2+	10G_PHY_MDC_SCL0
C47	DDI3_PAIR2-	10G_INT0
C48	RSVD	GND
C49	DDI3_PAIR3+	10G_KR_RX0+
C50	DDI3_PAIR3-	10G_KR_RX0-
C51	GND	GND
C52	PEG_RX0+	PCIE_RX16+
C53	PEG_RX0-	PCIE_RX16-
C54	TYPE0#	TYPE0#
C55	PEG_RX1+	PCIE_RX17+
C56	PEG_RX1-	PCIE_RX17-
C57	TYPE1#	TYPE1#
C58	PEG_RX2+	PCIE_RX18+
C59	PEG_RX2-	PCIE_RX18-
C60	GND	GND
C61	PEG_RX3+	PCIE_RX19+
C62	PEG_RX3-	PCIE_RX19-
C63	RSVD	RSVD
C64	RSVD	RSVD
C65	PEG_RX4+	PCIE_RX20+
C66	PEG_RX4-	PCIE_RX20-
C67	RAPID_SHUTDOWN	RAPID_SHUTDOWN
C68	PEG_RX5+	PCIE_RX21+
C69	PEG_RX5-	PCIE_RX21-
C70	GND	GND
C71	PEG_RX6+	PCIE_RX22+
C72	PEG_RX6-	PCIE_RX22-
C73	GND	GND
C74	PEG_RX7+	PCIE_RX23+

Pin	Type 6	Type 7
C75	PEG_RX7-	PCIE_RX23-
C76	GND	GND
C77	RSVD	RSVD
C78	PEG_RX8+	PCIE_RX24+
C79	PEG_RX8-	PCIE_RX24-
C80	GND	GND
C81	PEG_RX9+	PCIE_RX25+
C82	PEG_RX9-	PCIE_RX25-
C83	RSVD	RSVD
C84	GND	GND
C85	PEG_RX10+	PCIE_RX26+
C86	PEG_RX10-	PCIE_RX26-
C87	GND	GND
C88	PEG_RX11+	PCIE_RX27+
C89	PEG_RX11-	PCIE_RX27-
C90	GND	GND
C91	PEG_RX12+	PCIE_RX28+
C92	PEG_RX12-	PCIE_RX28-
C93	GND	GND
C94	PEG_RX13+	PCIE_RX29+
C95	PEG_RX13-	PCIE_RX29-
C96	GND	GND
C97	RSVD	RSVD
C98	PEG_RX14+	PCIE_RX30+
C99	PEG_RX14-	PCIE_RX30-
C100	GND	GND
C101	PEG_RX15+	PCIE_RX31+
C102	PEG_RX15-	PCIE_RX31-
C103	GND	GND
C104	VCC_12V	VCC_12V
C105	VCC_12V	VCC_12V
C106	VCC_12V	VCC_12V
C107	VCC_12V	VCC_12V
C108	VCC_12V	VCC_12V
C109	VCC_12V	VCC_12V
C110	GND	GND

Pin	Type 6	Type 7
D1	GND	GND
D2	GND	GND
D3	USB_SSTX0-	USB_SSTX0-
D4	USB_SSTX0+	USB_SSTX0+
D5	GND	GND
D6	USB_SSTX1-	USB_SSTX1-
D7	USB_SSTX1+	USB_SSTX1+
D8	GND	GND
D9	USB_SSTX2-	USB_SSTX2-
D10	USB_SSTX2+	USB_SSTX2+
D11	GND	GND
D12	USB_SSTX3-	USB_SSTX3-
D13	USB_SSTX3+	USB_SSTX3+
D14	GND	GND
D15	DDI1_CTRLCLK_AUX+	10G_PHY_MDIO_SDA3
D16	DDI1_CTRLDATA_AUX-	10G_PHY_MDIO_SDA2
D17	RSVD	10G_SDP3
D18	RSVD	GND
D19	PCIE_TX6+	PCIE_TX6+
D20	PCIE_TX6-	PCIE_TX6-
D21	GND	GND
D22	PCIE_TX7+	PCIE_TX7+
D23	PCIE_TX7-	PCIE_TX7-
D24	RSVD	10G_INT3
D25	RSVD	RSVD
D26	DDI1_PAIR0+	10G_KR_TX3+
D27	DDI1_PAIR0-	10G_KR_TX3-
D28	RSVD	GND
D29	DDI1_PAIR1+	10G_KR_TX2+
D30	DDI1_PAIR1-	10G_KR_TX2-
D31	GND	GND
D32	DDI1_PAIR2+	10G_SFP_SCL3
D33	DDI1_PAIR2-	10G_SFP_SCL2 -
D34	DDI1_DDC_AUX_SEL	10G_PHY_CAP_23
D35	RSVD	10G_PHY_CAP_01
D36	DDI1_PAIR3+	RSVD
D37	DDI1_PAIR3-	RSVD

Pin	Type 6	Type 7
D38	RSVD	10G_SFP_SCL1
D39	DDI2_PAIR0+	10G_SFP_SCL0
D40	DDI2_PAIR0-	10G_SDP1
D41	GND	GND
D42	DDI2_PAIR1+	10G_KR_TX1+
D43	DDI2_PAIR1-	10G_KR_TX1-
D44	DDI2_HPD	GND
D45	RSVD	10G_PHY_MDIO_SDA1
D46	DDI2_PAIR2+	10G_PHY_MDIO_SDA0
D47	DDI2_PAIR2-	10G_INT1
D48	RSVD	GND
D49	DDI2_PAIR3+	10G_KR_TX0+
D50	DDI2_PAIR3-	10G_KR_TX0-
D51	GND	GND
D52	PEG_TX0+	PCIE_TX16+
D53	PEG_TX0-	PCIE_TX16-
D54	PEG_LANE_RV#	RSVD
D55	PEG_TX1+	PCIE_TX17+
D56	PEG_TX1-	PCIE_TX17-
D57	TYPE2#	TYPE2#
D58	PEG_TX2+	PCIE_TX18+
D59	PEG_TX2-	PCIE_TX18-
D60	GND	GND
D61	PEG_TX3+	PCIE_TX19+
D62	PEG_TX3-	PCIE_TX19-
D63	RSVD	RSVD
D64	RSVD	RSVD
D65	PEG_TX4+	PCIE_TX20+
D66	PEG_TX4-	PCIE_TX20-
D67	GND	GND
D68	PEG_TX5+	PCIE_TX21+
D69	PEG_TX5-	PCIE_TX21-
D70	GND	GND
D71	PEG_TX6+	PCIE_TX22+
D72	PEG_TX6-	PCIE_TX22-
D73	GND	GND
D74	PEG_TX7+	PCIE_TX23+

Pin	Type 6	Type 7
D75	PEG_TX7-	PCIE_TX23-
D76	GND	GND
D77	RSVD	RSVD
D78	PEG_TX8+	PCIE_TX24+
D79	PEG_TX8-	PCIE_TX24-
D80	GND	GND
D81	PEG_TX9+	PCIE_TX25+
D82	PEG_TX9-	PCIE_TX25-
D83	RSVD	RSVD
D84	GND	GND
D85	PEG_TX10+	PCIE_TX26+
D86	PEG_TX10-	PCIE_TX26-
D87	GND	GND
D88	PEG_TX11+	PCIE_TX27+
D89	PEG_TX11-	PCIE_TX27-
D90	GND	GND
D91	PEG_TX12+	PCIE_TX28+
D92	PEG_TX12-	PCIE_TX28-
D93	GND	GND
D94	PEG_TX13+	PCIE_TX29+
D95	PEG_TX13-	PCIE_TX29-
D96	GND	GND
D97	RSVD	RSVD
D98	PEG_TX14+	PCIE_TX30+
D99	PEG_TX14-	PCIE_TX30-
D100	GND	GND
D101	PEG_TX15+	PCIE_TX31+
D102	PEG_TX15-	PCIE_TX31-
D103	GND	GND
D104	VCC_12V	VCC_12V
D105	VCC_12V	VCC_12V
D106	VCC_12V	VCC_12V
D107	VCC_12V	VCC_12V
D108	VCC_12V	VCC_12V
D109	VCC_12V	VCC_12V
D110	GND	GND

2. COM Express Mechanical Specification

2.1 COM Express Module Form Factors (Refer PICMG Module DG Rev.2.1)

Figure 2-1 Module Form Factors

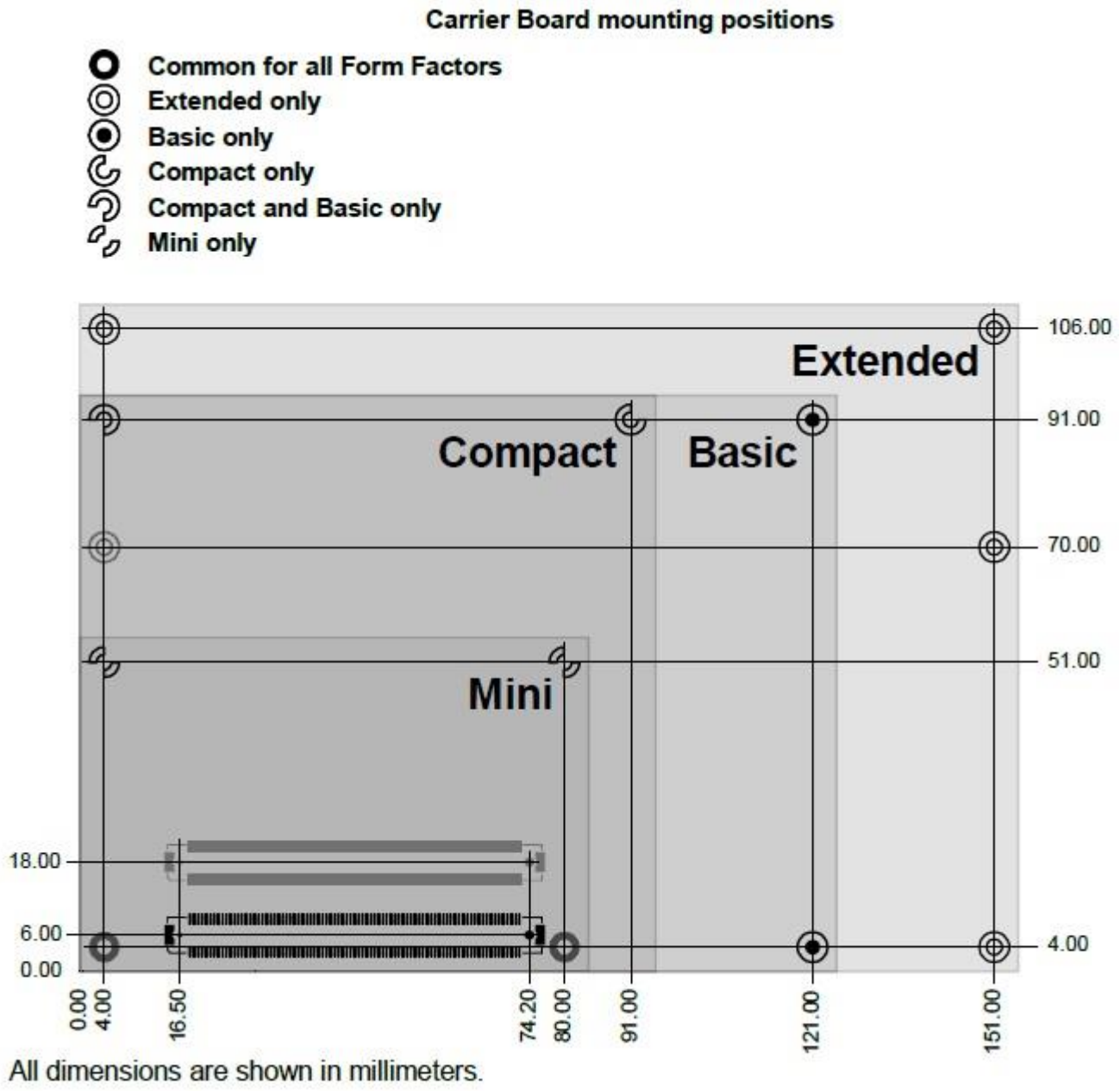
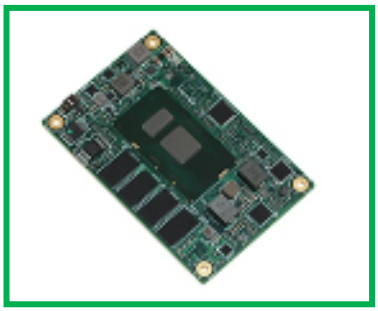


Figure 2-1-1 AAEON COM Express Module



Product: NanoCOM-SKU
COM Express Mini Type 10

Product: COM-SKU6
COM Express Compact Type 6

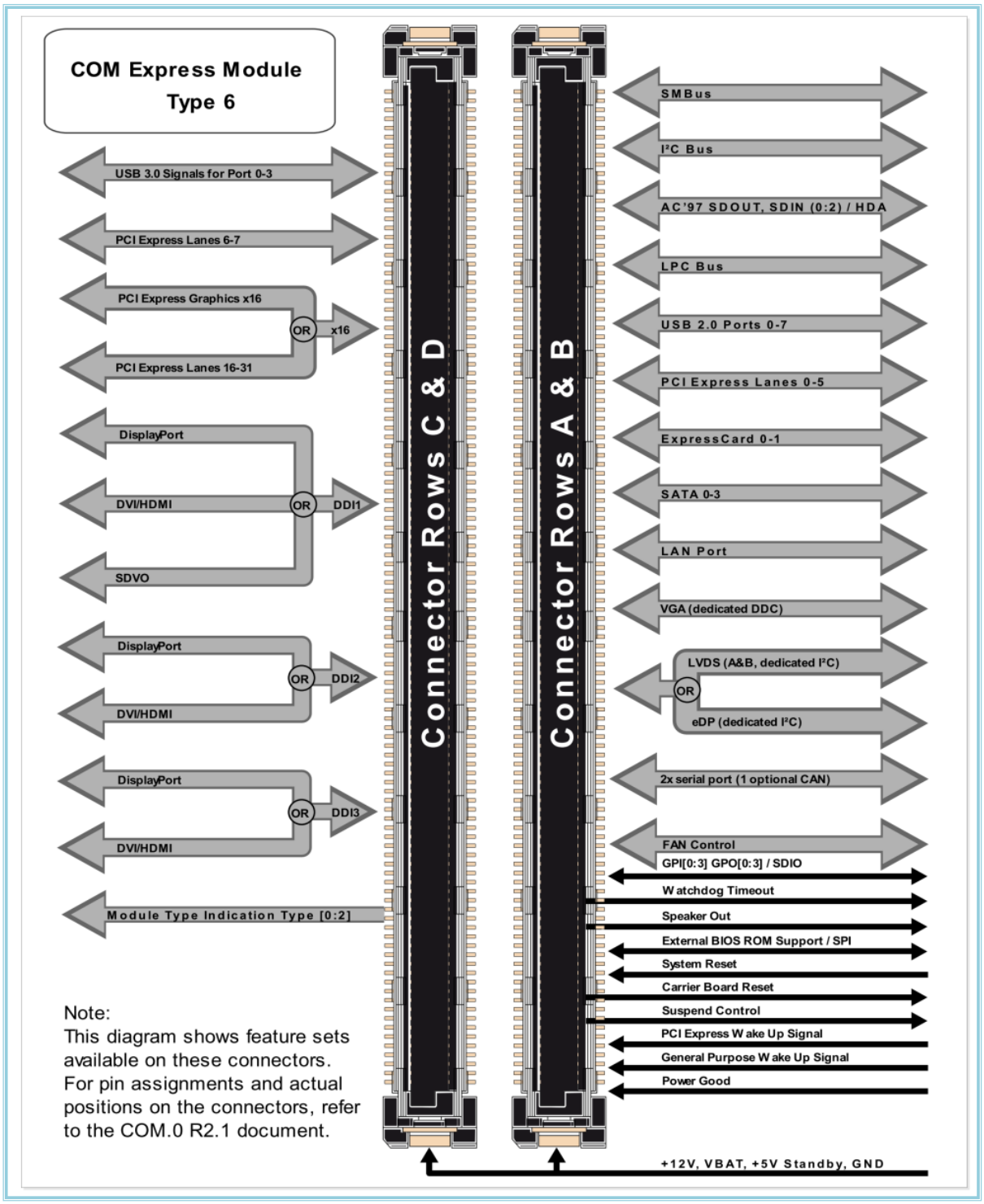
Product: COM-SKHB6
COM Express Basic Type 6

Product: COM-SKDB7
COM Express Compact Type 7

2.2 COM Express Connector

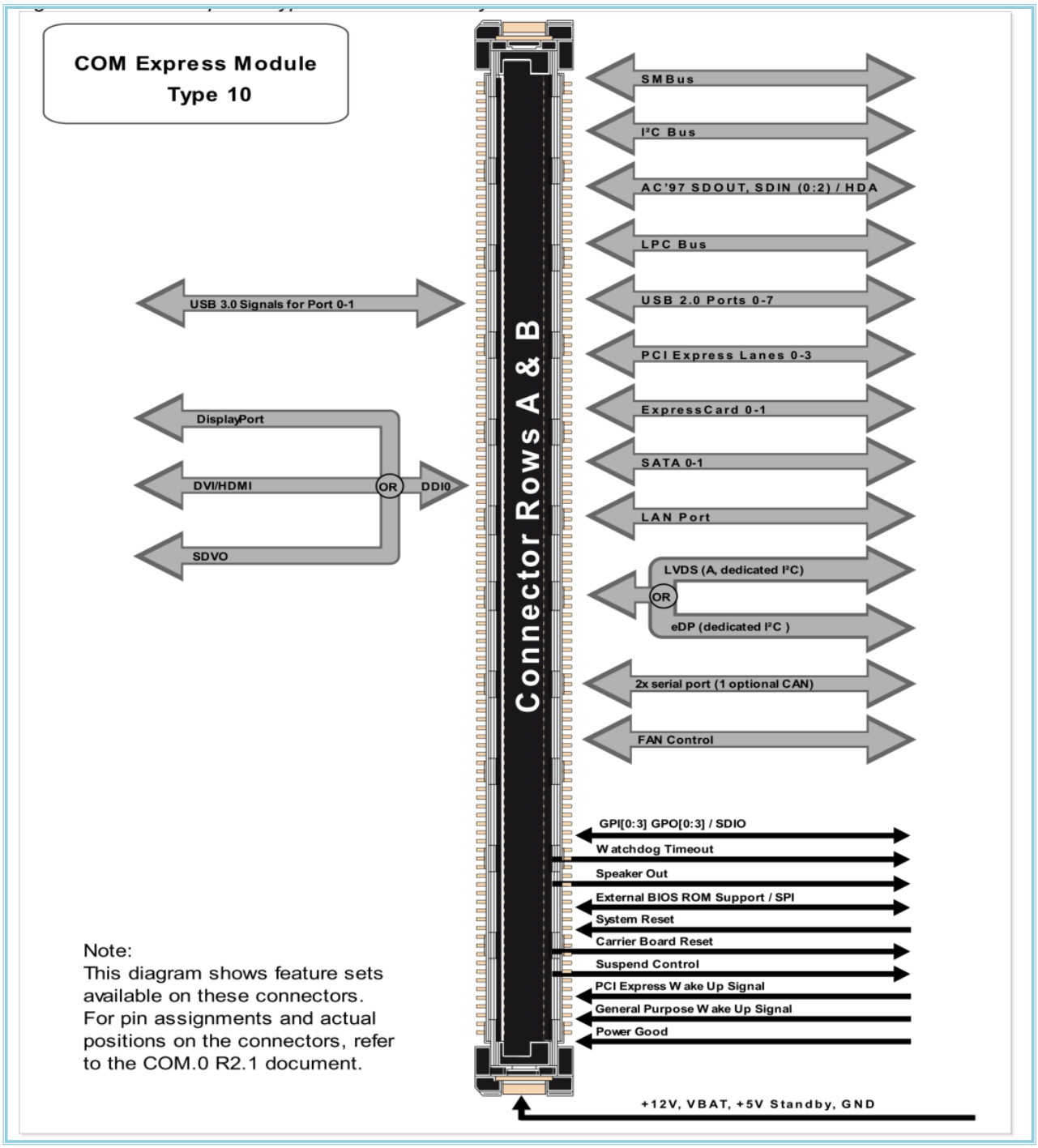
Type 6 of COM Express module utilizes two 220-pin high density connectors to interface the COM Express module and carrier board.

Figure 2-2 Type 6 ROW ABCD Connector



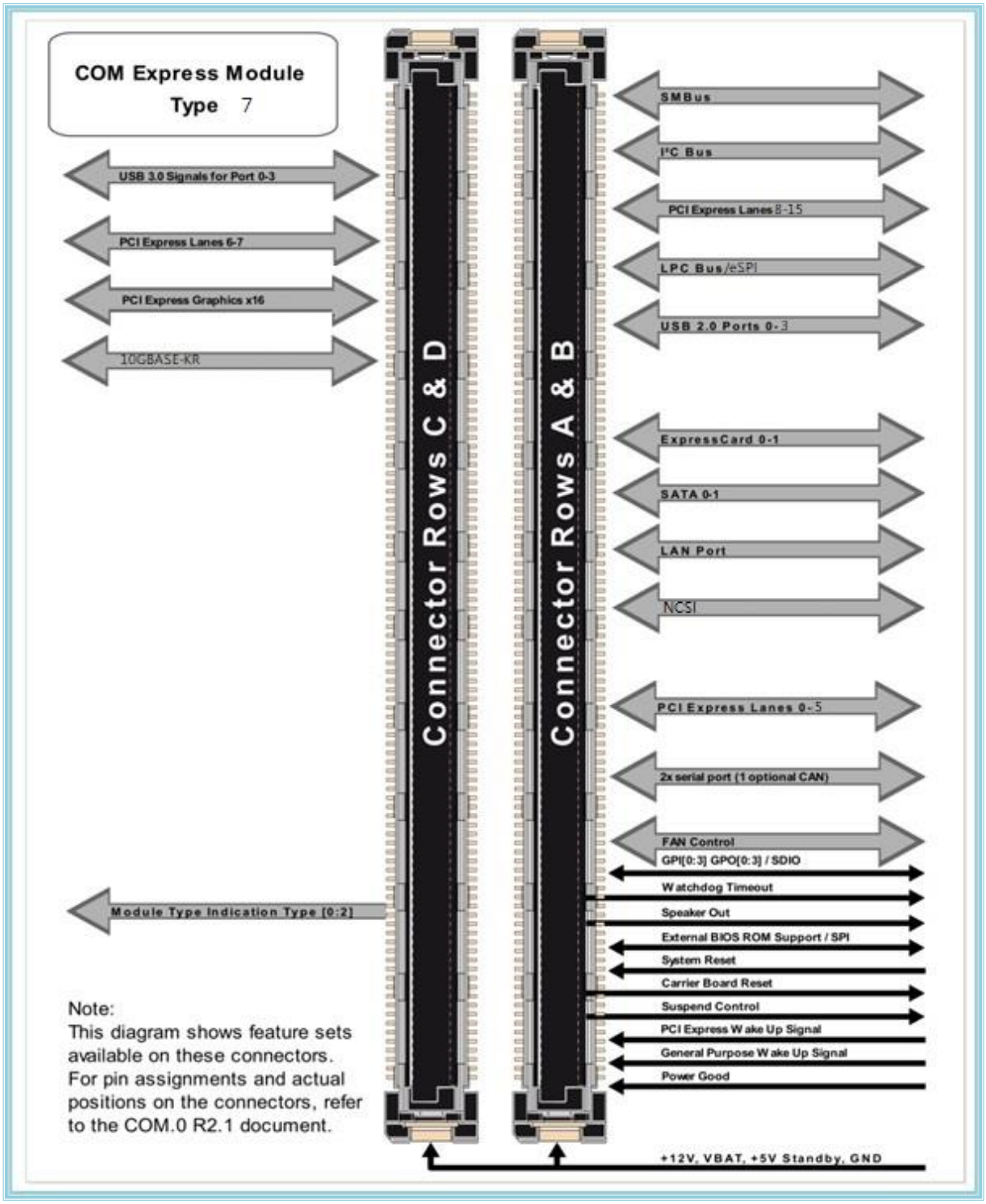
Type 10 of COM Express module utilizes one 220-pin high density connectors to interface the COM Express module and carrier board.

Figure 2-3 Type 10 ROW AB Connector



Type 7 of COM Express module utilizes two 220-pin high density connectors to interface the COM Express module and carrier board.

Figure 2-4 Type 7 ROW ABCD Connector



AAEON Connector Type :

Table 2-1: AAEON Connector Type

Connector Type	Height	Supplier - Model	AAEON's P/N
Carrier Board (Plug)	8 .0 mm	FOXCONN / QT002206-4131-3H	16540M0201
Module Board (Receptacle)	3.25 mm	FOXCONN / QT012206-1031-2H	16540M0001

Figure 2-5 Plug and Receptacle

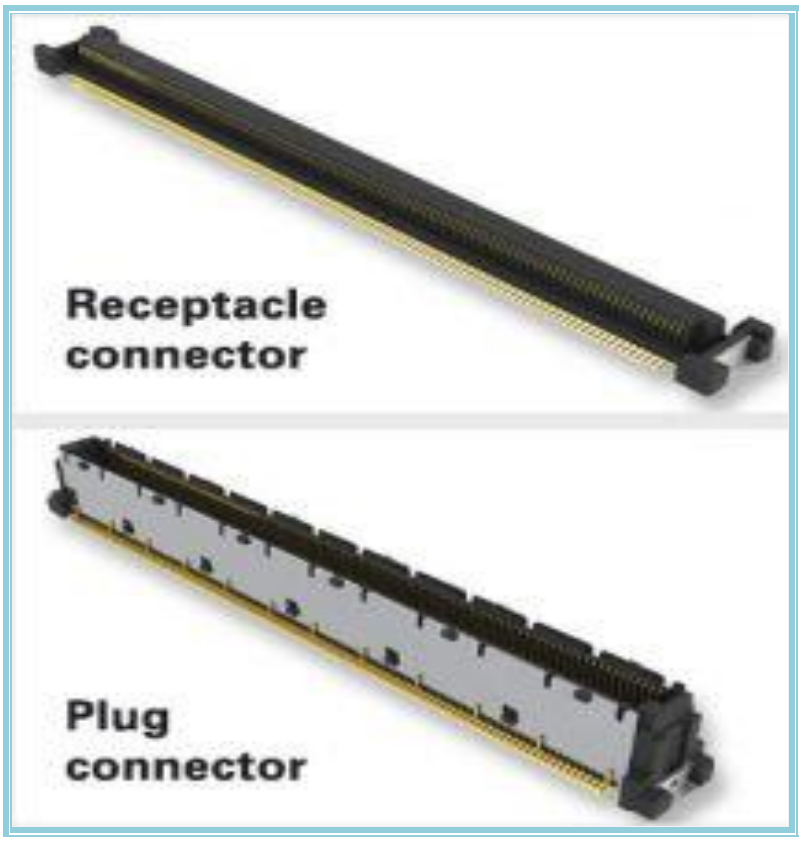
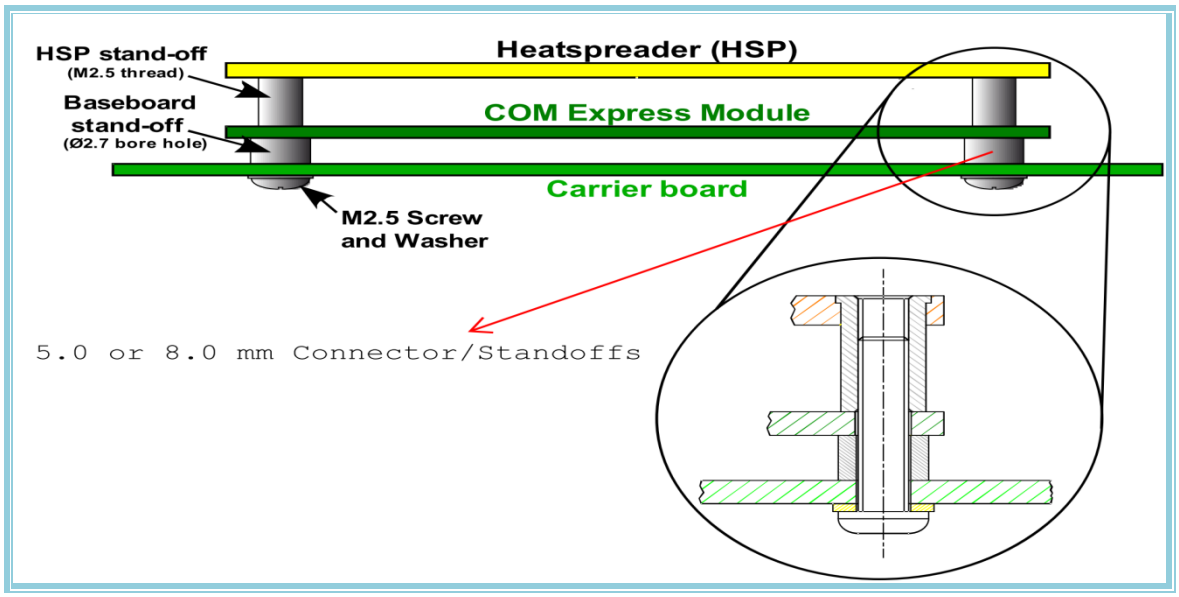


Figure 2-6 Heat spreader with Threaded Standoffs



3. Signal Description and Routing Guideline

3.1 PCB Stack Example

Table 3-1: PCB Stack Example

Layer	1	2	3	4	5	6	7	8	9	10	11	12	13	14
4	S1	G	P	S2										
4	S1	S2/G	P	S3										
4	S1	G	S2/P	S3										
6	S1	G	S2	S3	P	S4								
6	S1	S2/G	S3	S4	P	S5								
6	S1	G	S2	S3	P/S4	S5								
8	S1	G	S2	G	P	S3	G	S4						
8	S1	G	S2	S3	P	S4	G	S5						

Note : S=Signal routing layer , P=Power , G=Ground

3.2 General Layout rule : BY PLATFORM LAYOUT GUIDE

3.3 Interface Layout and Routing Recommendations

3.3.1 PCIE

PCI Express provides a scalable, high-speed, serial I/O point-to-point bus connection. PCIE is easy to work with, but design rules must be followed. The most important design rule is that the PCIE lanes must be routed as differential pairs.

3.3.1.1 Signal Definitions

Table 3-2: PCIE Signal Definitions

Pin	Type	Signal	Description	I/O
B68	Type 6,7	PCIE_RX0+	PCIE channel 0. Receive Input differential pair.	I PCIE
B69	Type 10	PCIE_RX0-		
A68	Type 6,7	PCIE_TX0+	PCIE channel 0. Transmit Output differential pair.	O PCIE
A69	Type 10	PCIE_TX0-		
B64	Type 6,7	PCIE_RX1+	PCIE channel 1. Receive Input differential pair.	I PCIE
B65	Type 10	PCIE_RX1-		
A64	Type 6,7	PCIE_TX1+	PCIE channel 1. Transmit Output differential pair.	O PCIE
A65	Type 10	PCIE_TX1-		
B61	Type 6,7	PCIE_RX2+	PCIE channel 2. Receive Input differential pair.	I PCIE
B62	Type 10	PCIE_RX2-		
A61	Type 6,7	PCIE_TX2+	PCIE channel 2. Transmit Output differential pair.	O PCIE
A62	Type 10	PCIE_TX2-		
B58	Type 6,7	PCIE_RX3+	PCIE channel 3. Receive Input differential pair.	I PCIE
B59	Type 10	PCIE_RX3-		
A58	Type 6,7	PCIE_TX3+	PCIE channel 3. Transmit Output differential pair.	O PCIE
A59	Type 10	PCIE_TX3-		
B55	Type 6	PCIE_RX4+	PCIE channel 4. Receive Input differential pair.	I PCIE
B56	Type 7	PCIE_RX4-		
A55	Type 6	PCIE_TX4+	PCIE channel 4. Transmit Output differential pair.	O PCIE
A56	Type 7	PCIE_TX4-		
B52	Type 6	PCIE_RX5+	PCIE channel 5. Receive Input differential pair.	I PCIE
B53	Type 7	PCIE_RX5-		
A52	Type 6	PCIE_TX5+	PCIE channel 5. Transmit Output differential pair.	O PCIE
A53	Type 7	PCIE_TX5-		
C19	Type 6	PCIE_RX6+	PCIE channel 6. Receive Input differential pair.	I PCIE
C20	Type 7	PCIE_RX6-		
D19	Type 6	PCIE_TX6+	PCIE channel 6. Transmit Output differential pair.	O PCIE
D20	Type 7	PCIE_TX6-		
C22	Type 6	PCIE_RX7+	PCIE channel 7. Receive Input differential pair.	I PCIE
C23	Type 7	PCIE_RX7-		

D22	Type 6	PCIE_TX7+	PCIE channel 7. Transmit Output differential pair.	O PCIE
D23	Type 7	PCIE_TX7-		
B71	Type 7	PCIE_RX8+	PCIE channel 8. Receive Input differential pair.	I PCIE
B72		PCIE_RX8-		
A71	Type 7	PCIE_TX8+	PCIE channel 8. Transmit Output differential pair.	O PCIE
A72		PCIE_TX8-		
B74	Type 7	PCIE_RX9+	PCIE channel 9. Receive Input differential pair.	I PCIE
B75		PCIE_RX9-		
A74	Type 7	PCIE_TX9+	PCIE channel 9. Transmit Output differential pair.	O PCIE
A75		PCIE_TX9-		
B77	Type 7	PCIE_RX10+	PCIE channel 10. Receive Input differential pair.	I PCIE
B78		PCIE_RX10-		
A77	Type 7	PCIE_TX10+	PCIE channel 10. Transmit Output differential pair.	O PCIE
A78		PCIE_TX10-		
B81	Type 7	PCIE_RX11+	PCIE channel 11. Receive Input differential pair.	I PCIE
B82		PCIE_RX11-		
A81	Type 7	PCIE_TX11+	PCIE channel 11. Transmit Output differential pair.	O PCIE
A82		PCIE_TX11-		
B39	Type 7	PCIE_RX12+	PCIE channel 12. Receive Input differential pair.	I PCIE
B40		PCIE_RX12-		
A39	Type 7	PCIE_TX12+	PCIE channel 12. Transmit Output differential pair.	O PCIE
A40		PCIE_TX12-		
B36	Type 7	PCIE_RX13+	PCIE channel 13. Receive Input differential pair.	I PCIE
B37		PCIE_RX13-		
A36	Type 7	PCIE_TX13+	PCIE channel 13. Transmit Output differential pair.	O PCIE
A37		PCIE_TX13-		
B25	Type 7	PCIE_RX14+	PCIE channel 14. Receive Input differential pair.	I PCIE
B26		PCIE_RX14-		
A25	Type 7	PCIE_TX14+	PCIE channel 14. Transmit Output differential pair.	O PCIE
A26		PCIE_TX14-		
B22	Type 7	PCIE_RX15+	PCIE channel 15. Receive Input differential pair.	I PCIE
B23		PCIE_RX15-		
A22	Type 7	PCIE_TX15+	PCIE channel 15. Transmit Output differential pair.	O PCIE
A23		PCIE_TX15-		
C52	Type 7	PCIE_RX16+	PCIE channel 16. Receive Input differential pair.	I PCIE
C53		PCIE_RX16-		
D52	Type 7	PCIE_TX16+	PCIE channel 16. Transmit Output differential pair.	O PCIE
D53		PCIE_TX16-		

C55	Type 7	PCIE_RX17+	PCIE channel 17. Receive Input	I PCIE
C56		PCIE_RX17-	differential pair.	
D55	Type 7	PCIE_TX17+	PCIE channel 17. Transmit Output	O PCIE
D56		PCIE_TX17-	differential pair.	
C58	Type 7	PCIE_RX18+	PCIE channel 18. Receive Input	I PCIE
C59		PCIE_RX18-	differential pair.	
D58	Type 7	PCIE_TX18+	PCIE channel 18. Transmit Output	O PCIE
D59		PCIE_TX18-	differential pair.	
C61	Type 7	PCIE_RX19+	PCIE channel 19. Receive Input	I PCIE
C62		PCIE_RX19-	differential pair.	
D61	Type 7	PCIE_TX19+	PCIE channel 19. Transmit Output	O PCIE
D62		PCIE_TX19-	differential pair.	
C65	Type 7	PCIE_RX20+	PCIE channel 20. Receive Input	I PCIE
C66		PCIE_RX20-	differential pair.	
D65	Type 7	PCIE_TX20+	PCIE channel 20. Transmit Output	O PCIE
D66		PCIE_TX20-	differential pair.	
C68	Type 7	PCIE_RX21+	PCIE channel 21. Receive Input	I PCIE
C69		PCIE_RX21-	differential pair.	
D68	Type 7	PCIE_TX21+	PCIE channel 21. Transmit Output	O PCIE
D69		PCIE_TX21-	differential pair.	
C71	Type 7	PCIE_RX22+	PCIE channel 22. Receive Input	I PCIE
C72		PCIE_RX22-	differential pair.	
D71	Type 7	PCIE_TX22+	PCIE channel 22. Transmit Output	O PCIE
D72		PCIE_TX22-	differential pair.	
C74	Type 7	PCIE_RX23+	PCIE channel 23. Receive Input	I PCIE
C75		PCIE_RX23-	differential pair.	
D74	Type 7	PCIE_TX23+	PCIE channel 23. Transmit Output	O PCIE
D75		PCIE_TX23-	differential pair.	
C78	Type 7	PCIE_RX24+	PCIE channel 24. Receive Input	I PCIE
C79		PCIE_RX24-	differential pair.	
D78	Type 7	PCIE_TX24+	PCIE channel 24. Transmit Output	O PCIE
D79		PCIE_TX24-	differential pair.	
C81	Type 7	PCIE_RX25+	PCIE channel 25. Receive Input	I PCIE
C82		PCIE_RX25-	differential pair.	
D81	Type 7	PCIE_TX25+	PCIE channel 25. Transmit Output	O PCIE
D82		PCIE_TX25-	differential pair.	
C85	Type 7	PCIE_RX26+	PCIE channel 26. Receive Input	I PCIE
C86		PCIE_RX26-	differential pair.	

D85	Type 7	PCIE_TX26+	PCIE channel 26. Transmit Output differential pair.	O PCIE
D86		PCIE_TX26-		
C88	Type 7	PCIE_RX27+	PCIE channel 27. Receive Input differential pair.	I PCIE
C89		PCIE_RX27-		
D88	Type 7	PCIE_TX27+	PCIE channel 27. Transmit Output differential pair.	O PCIE
D89		PCIE_TX27-		
C91	Type 7	PCIE_RX28+	PCIE channel 28. Receive Input differential pair.	I PCIE
C92		PCIE_RX28-		
D91	Type 7	PCIE_TX28+	PCIE channel 28. Transmit Output differential pair.	O PCIE
D92		PCIE_TX28-		
C94	Type 7	PCIE_RX29+	PCIE channel 29. Receive Input differential pair.	I PCIE
C95		PCIE_RX29-		
D94	Type 7	PCIE_TX29+	PCIE channel 29. Transmit Output differential pair.	O PCIE
D95		PCIE_TX29-		
C98	Type 7	PCIE_RX30+	PCIE channel 30. Receive Input differential pair.	I PCIE
C99		PCIE_RX30-		
D98	Type 7	PCIE_TX30+	PCIE channel 30. Transmit Output differential pair.	O PCIE
D99		PCIE_TX30-		
C101	Type 7	PCIE_RX31+	PCIE channel 31. Receive Input differential pair.	I PCIE
C102		PCIE_RX31-		
D101	Type 7	PCIE_TX31+	PCIE channel 31. Transmit Output differential pair.	O PCIE
D102		PCIE_TX31-		
A88	Type 6,7 Type 10	PCIE_CLK_REF+	PCIE Reference Clock for all COM Express PCIE lanes, and for PEG lanes.	O PCIE
A89		PCIE_CLK_REF-		
A49	Type 6,7 Type 10	GBE0_SDP	Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.	IO
A48	Type 6,7 Type 10	RSVD		
B48	Type 6,7 Type 10	USB0_HOST_PRSNT	Module USB client may detect the presence of a USB host on USB0. A high value indicates that a host is present.	I CMOS
B47	Type 6,7 Type 10	ESPI_EN#	This signal is used by the Carrier to indicate the operating mode of the LPC/eSPI bus. If left unconnected on the carrier, LPC mode (default) is selected. If pulled to GND on the carrier, eSPI mode is selected. This	O CMOS

			signal is pulled to a logic high on the module through a resistor. The Carrier should only float this line or pull it Low.	
B50	Type 6,7 Type 10	CB_RESET#	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.	O CMOS
B66	Type 6,7 Type 10	WAKE0#	PCI Express wake up signal	I CMOS

3.3.1.2 PCIE Reference Schematics

Figure 3-1 PCIE[x1] Reference Schematic

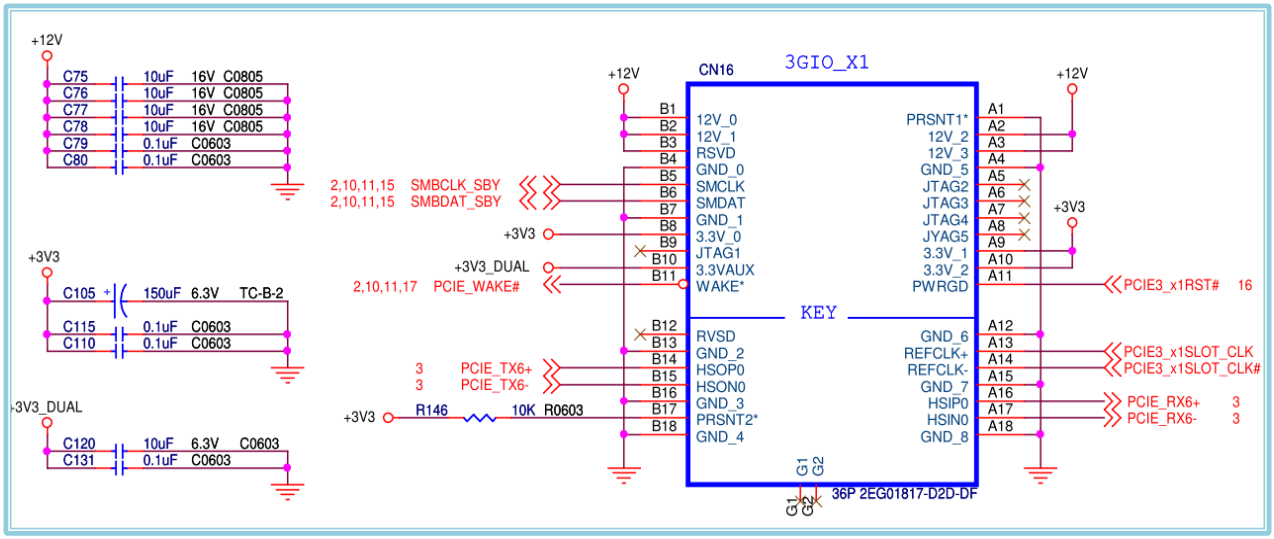


Figure 3-2 Mini-Card for mSATA / PCIE Switching Reference Schematic

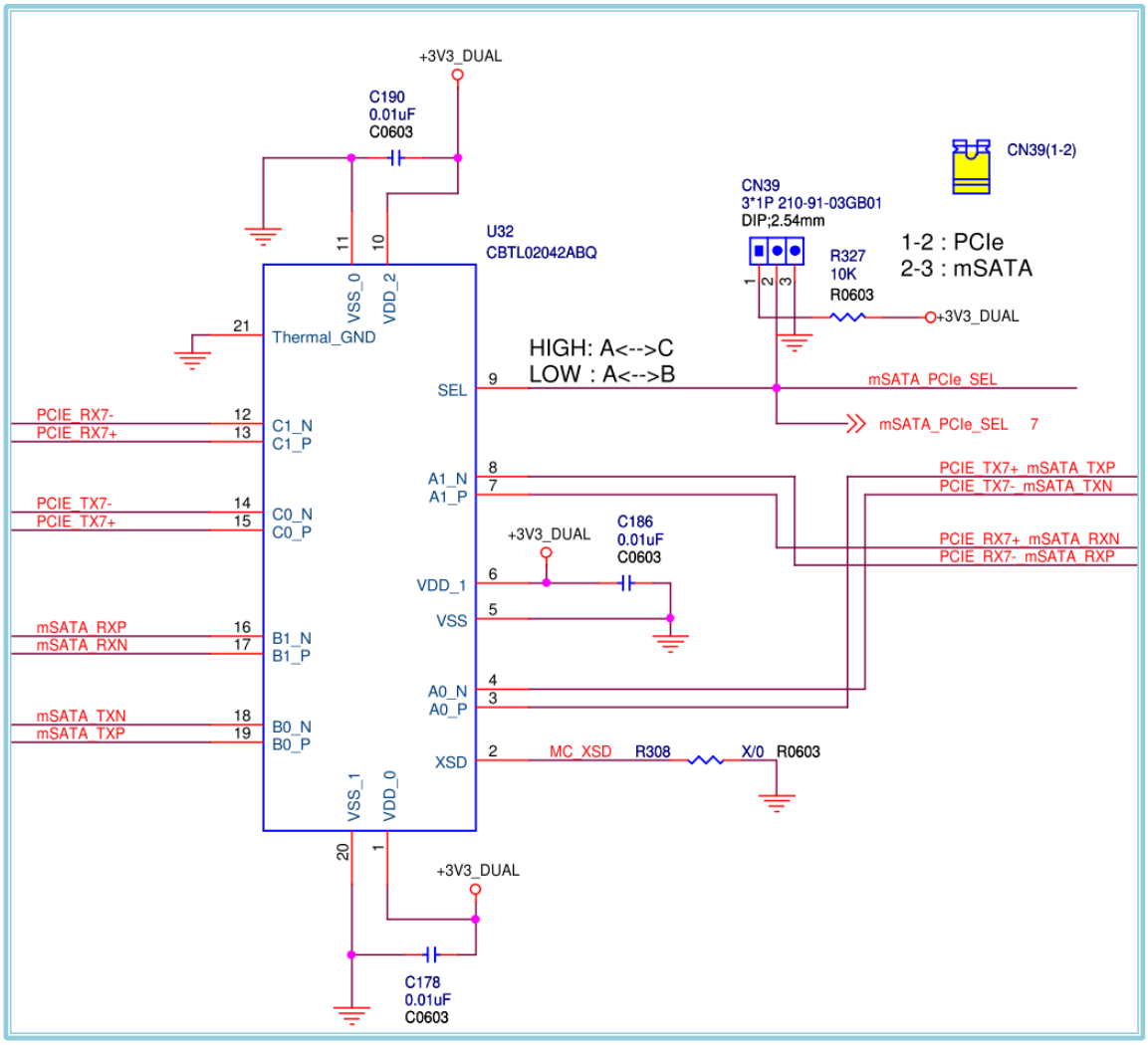
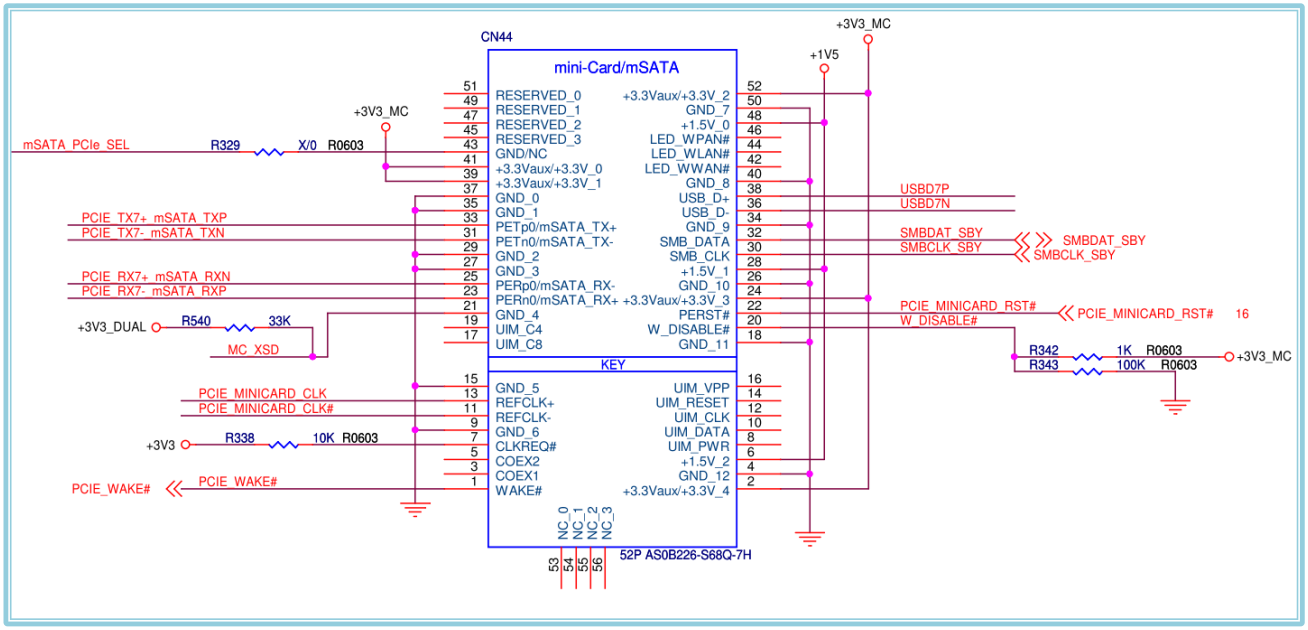


Figure 3-3 Mini-Card for mSATA / PCIE Reference Schematic



3.3.1.3 PCIE Layout Recommendations

Table 3-3: PCIE / PEG Trace Routing Guidelines

Parameter	PCIE Gen1	PCIE Gen2	PCIE Gen3
Symbol Rate	2.5 G	5.0 G	8.0 G
Carrier Board Signal length (to PCIE slot)	9.0 inches	9.0 inches	4.0 inches a redriver may be necessary for GEN3 signaling rates
Differential impedance	85 Ω +/-15% (Impedence may vary when different platform used)		
Single-ended Impedance	55 Ω +/-15%	50 Ω +/-15%	50 Ω +/-15%
Trace width / Spacing between differential pairs	PCB stack-up dependent		
Spacing between RX and TX (inter-pair) / differential pairs and low-speed non periodic signals	Min. 20mils		
Spacing between differential pairs and high-speed periodic signals	Min. 50mils		
Length matching between differential pairs (intra-pair)	Max. 5mils		
Reference plane	GND referenced preferred		
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements.Keep difference within a 3.0 inch delta to minimize latency.		
Via Usage	Max. 2 vias per TX trace Max. 4 vias per RX trace		Max. 2 vias per TX trace Max. 2 vias per RX trace
AC coupling capacitors	Capacitor type: X7R, 100nF +/- 10%, 16V, shape 0402.		

3.3.2 PEG

The PEG Port can utilize COM Express PCIE lanes 16-32 to drive a x16 link for an external high-performance PCI Express Graphics card. Type 6 provides dedicated PEG and SDVO channels.

3.3.2.1 Signal Definitions

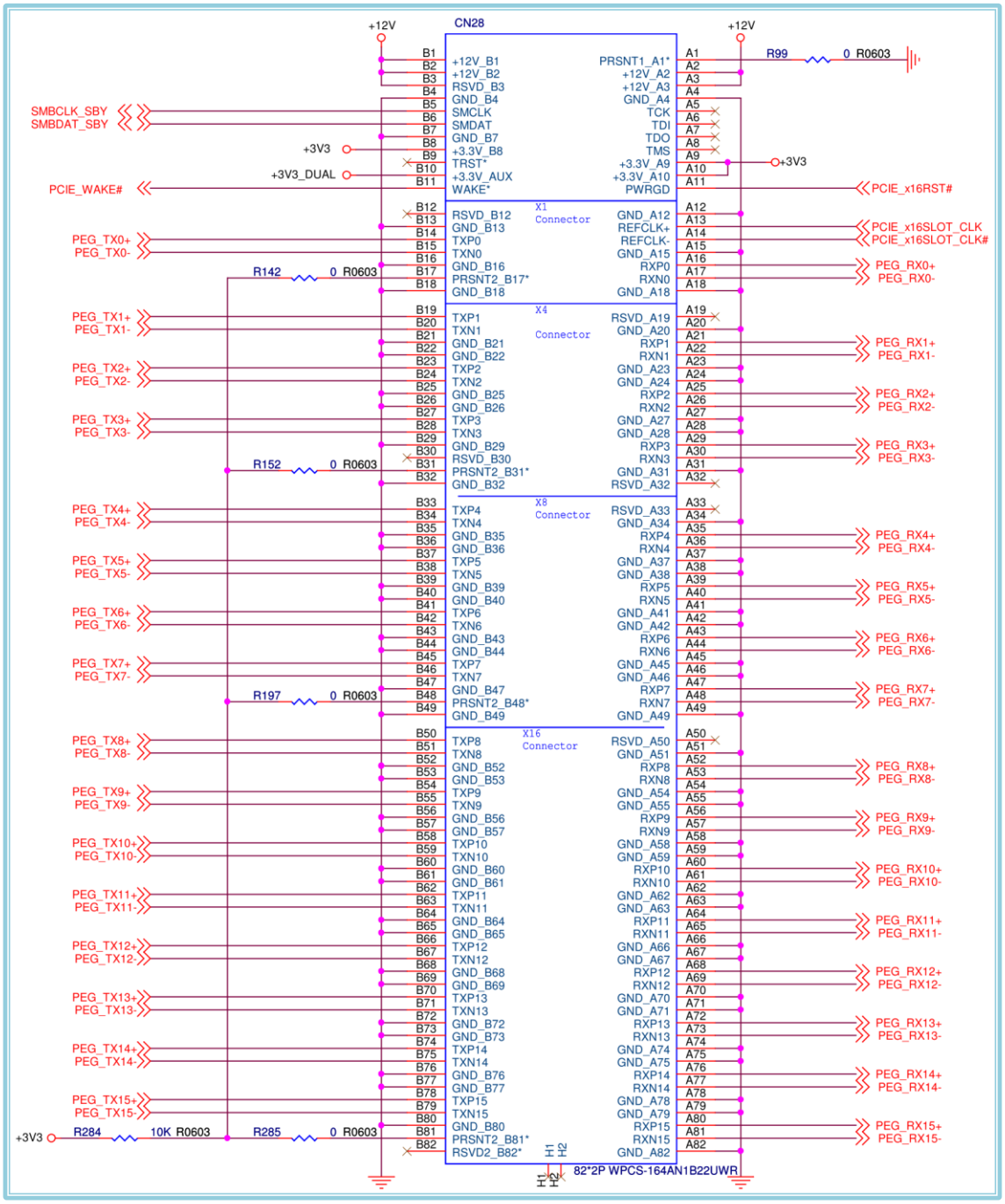
Table 3-4: PEG Signal Definitions

Pin	Type	Signal	Description	I/O
C52	Type 6	PEG_RX0+	PEG channel 0, Receive Input differential pair.	I PCIE
C53		PEG_RX0-		
D52	Type 6	PEG_TX0+	PEG channel 0, Transmit Output differential pair.	O PCIE
D53		PEG_TX0-		
C55	Type 6	PEG_RX1+	PEG channel 1, Receive Input differential pair.	I PCIE
C56		PEG_RX1-		
D55	Type 6	PEG_TX1+	PEG channel 1, Transmit Output differential pair.	O PCIE
D56		PEG_TX1-		
C58	Type 6	PEG_RX2+	PEG channel 2, Receive Input differential pair.	I PCIE
C59		PEG_RX2-		
D58	Type 6	PEG_TX2+	PEG channel 2, Transmit Output differential pair.	O PCIE
D59		PEG_TX2-		
C61	Type 6	PEG_RX3+	PEG channel 3, Receive Input differential pair.	I PCIE
C62		PEG_RX3-		
D61	Type 6	PEG_TX3+	PEG channel 3, Transmit Output differential pair.	O PCIE
D62		PEG_TX3-		
C65	Type 6	PEG_RX4+	PEG channel 4, Receive Input differential pair.	I PCIE
C66		PEG_RX4-		
D65	Type 6	PEG_TX4+	PEG channel 4, Transmit Output differential pair.	O PCIE
D66		PEG_TX4-		
C68	Type 6	PEG_RX5+	PEG channel 5, Receive Input differential pair.	I PCIE
C69		PEG_RX5-		
D68	Type 6	PEG_TX5+	PEG channel 5, Transmit Output differential pair.	O PCIE
D69		PEG_TX5-		
C71	Type 6	PEG_RX6+	PEG channel 6, Receive Input differential pair.	I PCIE
C72		PEG_RX6-		
D71	Type 6	PEG_TX6+	PEG channel 6, Transmit Output differential pair.	O PCIE
D72		PEG_TX6-		
C74	Type 6	PEG_RX7+	PEG channel 7, Receive Input differential pair.	I PCIE
C75		PEG_RX7-		
D74	Type 6	PEG_TX7+	PEG channel 7, Transmit Output differential pair.	O PCIE
D75		PEG_TX7-		

C78	Type 6	PEG_RX8+	PEG channel 8, Receive Input differential pair.	I PCIE
C79		PEG_RX8-		
D78	Type 6	PEG_TX8+	PEG channel 8, Transmit Output differential pair.	O PCIE
D79		PEG_TX8-		
C81	Type 6	PEG_RX9+	PEG channel 9, Receive Input differential pair.	I PCIE
C82		PEG_RX9-		
D81	Type 6	PEG_TX9+	PEG channel 9, Transmit Output differential pair.	O PCIE
D82		PEG_TX9-		
C85	Type 6	PEG_RX10+	PEG channel 10, Receive Input differential pair.	I PCIE
C86		PEG_RX10-		
D85	Type 6	PEG_TX10+	PEG channel 10, Transmit Output differential pair.	O PCIE
D86		PEG_TX10-		
C88	Type 6	PEG_RX11+	PEG channel 11, Receive Input differential pair.	I PCIE
C89		PEG_RX11-		
D88	Type 6	PEG_TX11+	PEG channel 11, Transmit Output differential pair.	O PCIE
D89		PEG_TX11-		
C91	Type 6	PEG_RX12+	PEG channel 12, Receive Input differential pair.	I PCIE
C92		PEG_RX12-		
D91	Type 6	PEG_TX12+	PEG channel 12, Transmit Output differential pair.	O PCIE
D92		PEG_TX12-		
C94	Type 6	PEG_RX13+	PEG channel 13, Receive Input differential pair.	I PCIE
C95		PEG_RX13-		
D94	Type 6	PEG_TX13+	PEG channel 13 Transmit Output differential pair.	O PCIE
D95		PEG_TX13-		
C98	Type 6	PEG_RX14+	PEG channel 14, Receive Input differential pair.	I PCIE
C99		PEG_RX14-		
D98	Type 6	PEG_TX14+	PEG channel 14, Transmit Output differential pair.	O PCIE
D99		PEG_TX14-		
C101	Type 6	PEG_RX15+	PEG channel 15, Receive Input differential pair.	I PCIE
C102		PEG_RX15-		
D101	Type 6	PEG_TX15+	PEG channel 15, Transmit Output differential pair.	O PCIE
D102		PEG_TX15-		
D54	Type 6	PEG_LANE_RV#	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.	I 3.3V CMOS
A88	Type 6 Type 10	PCIE_CLK_REF+	PCIE Reference Clock for all COM Express PCIE lanes, and for PEG lanes	O CMOS
A89		PCIE_CLK_REF-		

3.3.2.2 PEG Reference Schematics

Figure 3-4 PEG Reference Schematic



3.3.2.3 PEG Layout Recommendations

(Refer 3.3.1.3)

3.3.3 LAN

All COM Express Modules provide at least one LAN port. The 8-wire 10/100/1000BaseT Gigabit Ethernet interface compliant to the IEEE 802.3-2005 specification is the preferred interface for this port, with the COM Express Module PHY responsible for implementing auto-negotiation of 10/100BaseTX vs 10/100/1000BaseT operation.

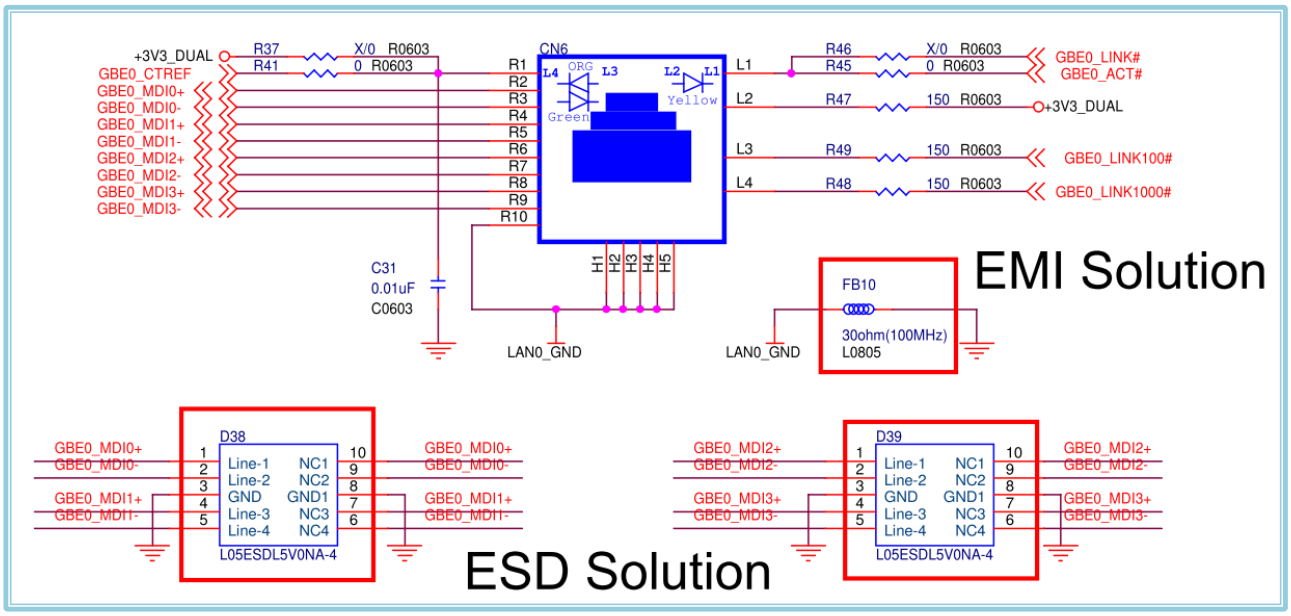
3.3.3.1 Signal Definitions

Table 3-5: LAN Signal Definitions

Pin	Type	Signal	Description	I/O
A2	Type 6,7	GBE0_MDI3-	Media Dependent Interface (MDI) differential pair 3. The	I/O GBE
A3	Type 10	GBE0_MDI3+	MDI can operate in 1000, 100, and 10Mbit/sec modes.	
A4	Type 6,7	GBE0_LINK100#	Ethernet controller 0 100Mbit/sec link indicator, active low.	O 3.3V Suspend
A5	Type 10	GBE0_LINK1000#	Ethernet controller 0 1000Mbit/sec link indicator, active low.	OD CMOS
A6	Type 6,7	GBE0_MDI2-	Media Dependent Interface (MDI) differential pair 2. The	I/O GBE
A7	Type 10	GBE0_MDI2+	MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE
A8	Type 6,7	GBE0_LINK#	Ethernet controller 0 link indicator, active low.	O 3.3V Suspend
B2	Type 10	GBE0_ACT#	Ethernet controller 0 activity indicator, active low.	OD CMOS
A9	Type 6,7	GBE0_MDI1-	Media Dependent Interface (MDI) differential pair 1. The	I/O GBE
A10	Type 10	GBE0_MDI1+	MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE
A12	Type 6,7	GBE0_MDI0-	Media Dependent Interface (MDI) differential pair 0. The	I/O GBE
A13	Type 10	GBE0_MDI0+	MDI can operate in 1000, 100, and 10Mbit/sec modes.	I/O GBE
A14	Type 6,7 Type 10	GBE0_CTREF	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.	REF

3.3.3.2 LAN Reference Schematics

Figure 3-5 RJ45 Reference Schematic



Note : TVS placement must be close to Connector for ESD Solution .

3.3.3.3 LAN Layout Recommendations

Table 3-6: LAN Trace Routing Guidelines

Parameter	Trace Routing
Carrier Board Signal length	5.0 inches
Max signal length between isolation magnetics Module and RJ45 connector	1.0 inch
Differential Impedance	95 Ω +/-20% (Impedence may vary when different LAN IC)
Single-ended Impedance	55 Ω +/-15%
Trace width / Differential pairs Spacing (intra-pair)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair)	Min. 50mils
Spacing between differential pairs and high-speed periodic signals	Min. 300mils
Spacing between differential pairs and low-speed non periodic signals	Min. 100mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	Max. 30mils
Spacing between digital ground and analog ground plane (between the magnetics Module and RJ45 connector)	Min. 60mils
Spacing from edge of plane	Min. 40mils
Via Usage	Max. of 2 vias on TX path Max. of 2 vias on RX path

3.3.4 USB

All USB interfaces shall be USB 2.0 compliant. There are 4 over-current signals shared by the 8 USB Ports. A Carrier must current limit the USB power source to minimize disruption of the Carrier in the event that a short or over-current condition exists on one of the USB Ports. A Module must fill the USB Ports starting at Port 0.

3.3.4.1 Signal Definitions

Table 3-7: USB2.0 Signal Definitions

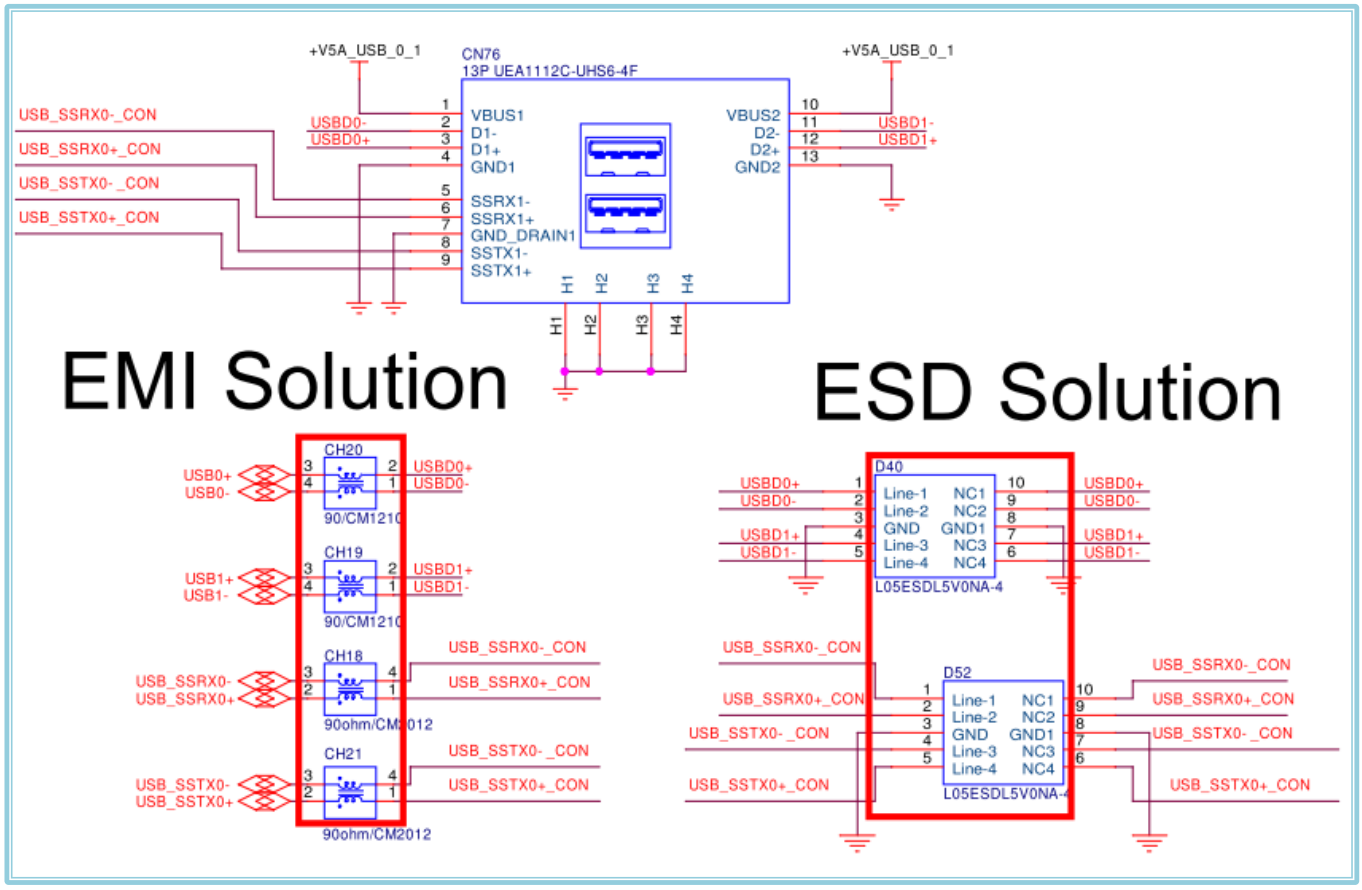
Pin	Type	Signal	Description	I/O
A46	Type 6,7	USB0+	USB Port 0, data + or D+, mandatory on Module	I/O USB
A45	Type 10	USB0-	USB Port 0, data - or D-, mandatory on Module	I/O USB
B46	Type 6,7	USB1+	USB Port 1, data + or D+, mandatory on Module	I/O USB
B45	Type 10	USB1-	USB Port 1, data - or D-, mandatory on Module	I/O USB
A43	Type 6,7	USB2+	USB Port 2, data + or D+, mandatory on Module	I/O USB
A42	Type 10	USB2-	USB Port 2, data - or D-, mandatory on Module	I/O USB
B43	Type 6,7	USB3+	USB Port 3, data + or D+, mandatory on Module	I/O USB
B42	Type 10	USB3-	USB Port 3, data - or D-, mandatory on Module	I/O USB
A40	Type 6	USB4+	USB Port 4, data + or D+, optional on Module	I/O USB
A39	Type 10	USB4-	USB Port 4, data - or D-, optional on Module	I/O USB
B40	Type 6	USB5+	USB Port 5, data + or D+, optional on Module	I/O USB
B39	Type 10	USB5-	USB Port 5, data - or D-, optional on Module	I/O USB
A37	Type 6	USB6+	USB Port 6, data + or D+, optional on Module	I/O USB
A36	Type 10	USB6-	USB Port 6, data - or D-, optional on Module	I/O USB
B37	Type 6	USB7+	USB Port 7, data + or D+, optional on Module	I/O USB
B36	Type 10	USB7-	USB Port 7, data - or D-, optional on Module	I/O USB
B44	Type 6,7	USB_0_1_OC#	USB over-current sense, USB ports 0 and 1. optional on Module	I 3.3V CMOS
A44	Type 10	USB_2_3_OC#	USB over-current sense, USB ports 2 and 3. optional on Module	I 3.3V CMOS
B38	Type 6	USB_4_5_OC#	USB over-current sense, USB ports 4 and 5. optional on Module	I 3.3V CMOS
A38	Type 10	USB_6_7_OC#	USB over-current sense, USB ports 6 and 7. optional on Module	I 3.3V CMOS

Table 3-8: USB3.0 Signal Definitions

Pin	Type	Signal	Description	I/O
D4	Type 6,7	**USB_SSTX0+**	USB Port 0, SuperSpeed TX +	O PCIE
B23	Type 10			
D3	Type 6,7	**USB_SSTX0-**	USB Port 0, SuperSpeed TX -	O PCIE
B22	Type 10			
D7	Type 6,7	**USB_SSTX1+**	USB Port 1, SuperSpeed TX +	O PCIE
B26	Type 10			
D6	Type 6,7	**USB_SSTX1-**	USB Port 1, SuperSpeed TX -	O PCIE
B25	Type 10			
D10	Type 6,7	USB_SSTX2+	USB Port 2, SuperSpeed TX +	O PCIE
D9	Type 6,7	USB_SSTX2-	USB Port 2, SuperSpeed TX -	O PCIE
D13	Type 6,7	USB_SSTX3+	USB Port 3, SuperSpeed TX +	O PCIE
D12	Type 6,7	USB_SSTX3-	USB Port 3, SuperSpeed TX -	O PCIE
C4	Type 6,7	**USB_SSRX0+**	USB Port 0, SuperSpeed RX +	I PCIE
A23	Type 10			
C3	Type 6,7	**USB_SSRX0-**	USB Port 0, SuperSpeed RX -	I PCIE
A22	Type 10			
C7	Type 6,7	**USB_SSRX1+**	USB Port 1, SuperSpeed RX +	I PCIE
A26	Type 10			
C6	Type 6,7	**USB_SSRX1-**	USB Port 1, SuperSpeed RX -	I PCIE
A25	Type 10			
C10	Type 6,7	USB_SSRX2+	USB Port 2, SuperSpeed RX +	I PCIE
C9	Type 6,7	USB_SSRX2-	USB Port 2, SuperSpeed RX -	I PCIE
C13	Type 6,7	USB_SSRX3+	USB Port 3, SuperSpeed RX +	I PCIE
C12	Type 6,7	USB_SSRX3-	USB Port 3, SuperSpeed RX -	I PCIE

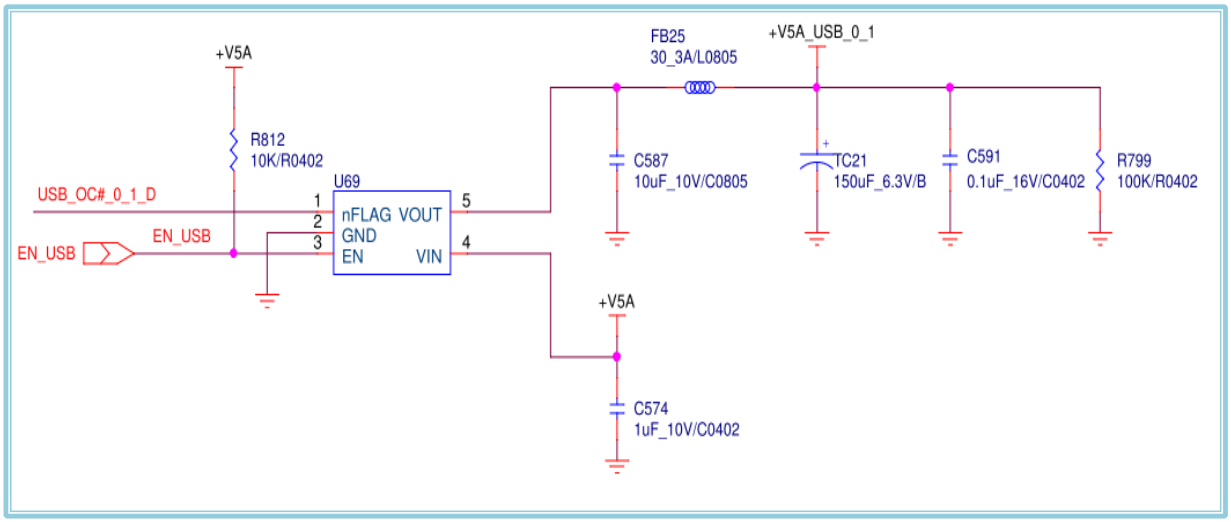
3.3.4.2 USB Reference Schematics - USB2.0 & USB3.0

Figure 3-6 USB2.0+USB3.0 Reference Schematic



Note : TVS placement must be close to Connector for ESD Solution .

Figure 3-7 USB Power Over-Current Protection Reference Schematic



3.3.4.3 USB Layout Recommendations

Table 3-9: USB2.0 and USB3.0 Trace Routing Guidelines

Parameter	USB2.0 Trace Routing	USB3.0 Trace Routing
Transfer rate	480 MBit/s	5.0 GBit/s
Maximum signal line length	Max. 17.0 inches	7.5 inches
Carrier Board Signal length	14.0 inches	4.5 inches
Differential Impedance	90 Ω +/-15% (Impedence may vary when different platform used)	85 Ω +/-10% (Impedence may vary when different platform used)
Single-ended Impedance	45 Ω +/-10%	50 Ω +/-15%
Trace width / differential pairs Spacing (intra-pair)	PCB stack-up dependent	PCB stack-up dependent
Spacing between pairs-to-pairs (inter-pair)	Min. 20mils	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils	Min. 20mils
Length matching between differential pairs (intra-pair)	150mils	Max. 5mils
Reference plane	Ground	Ground
Spacing from edge of plane	Min. 40mils	
Via Usage	Try to minimize number of vias (Max. 3 vias per differential signal trace)	

3.3.5 SATA

Serial ATA links for support of existing SATA Gen1, 2 and 3 devices.

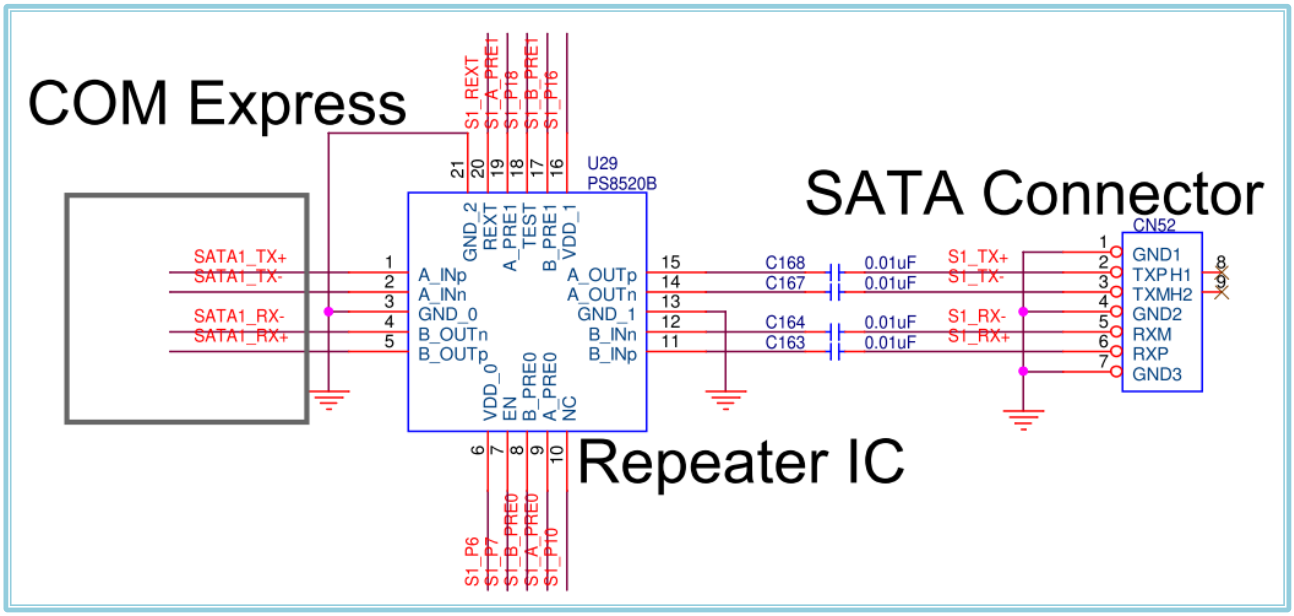
3.3.5.1 Signal Definitions

Table 3-10: SATA Signal Definitions

Pin	Type	Signal	Description	I/O
A16	Type 6,7	SATA0_TX+	SATA channel 0	O SATA
A17	Type 10	SATA0_TX-	Transmit output differential pair.	
A19	Type 6,7	SATA0_RX+	SATA channel 0	I SATA
A20	Type 10	SATA0_RX-	Receive input differential pair.	
B16	Type 6,7	SATA1_TX+	SATA channel 1	O SATA
B17	Type 10	SATA1_TX-	Transmit output differential pair.	
B19	Type 6,7	SATA1_RX+	SATA channel 1	I SATA
B20	Type 10	SATA1_RX-	Receive input differential pair.	
A22	Type 6	SATA2_TX+	SATA channel 2	O SATA
A23		SATA2_TX-	Transmit output differential pair.	
A25	Type 6	SATA2_RX+	SATA channel 2	I SATA
A26		SATA2_RX-	Receive input differential pair.	
B22	Type 6	SATA3_TX+	SATA channel 3	O SATA
B23		SATA3_TX-	Transmit output differential pair.	
B25	Type 6	SATA3_RX+	SATA channel 3	I SATA
B26		SATA3_RX-	Receive input differential pair.	
A28	Type 6,7 Type 10	SATA_ACT#	SATA activity LED. Open collector output pin driven during SATA command activity.	O 3.3V CMOS OC

3.3.5.2 SATA Reference Schematics

Figure 3-8 SATA (with Repeater IC) Reference Schematic



Note: Please contact repeater IC vendor FAE for high-quality SATA electrical signals.

3.3.5.3 SATA Layout Recommendations

Table 3-11: SATA Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	Up to 6.0 GBit/s
Maximum signal line length	5.0 inches
Carrier Board Signal length	3 inches
	a redriver may be necessary for GEN3 signaling rates
Differential Impedance	85 Ω +/-20% (Impedence may vary when different platform used)
Single-ended Impedance	50 Ω +/-15%
Trace width / differential pairs Spacing (intra-pair)	PCB stack-up dependent
Spacing between RX and TX pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between RX and TX pairs (inter-pair)	No strict length-matching requirements.
Spacing from edge of plane	Min. 40mils
Via Usage	maximum of 2 vias

3.3.6 LVDS

Each COM Express LVDS channel consists of four differential data pairs and a differential clock pair for a total of five differential pairs per channel. COM Express Modules and Module chipsets may not use all pairs.

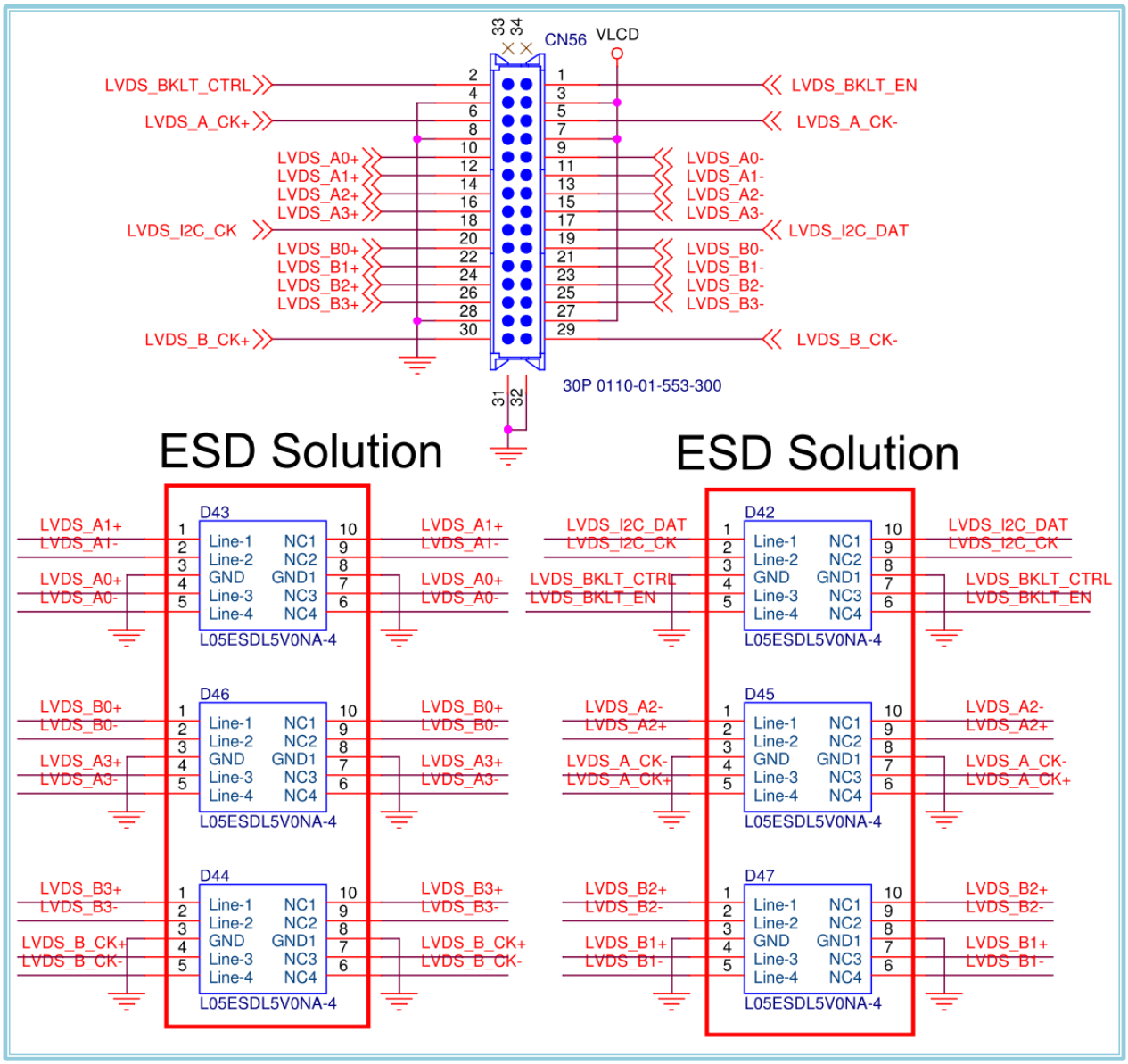
3.3.6.1 Signal Definitions

Table 3-12: LVDS Signal Definitions

Pin	Type	Signal	Description	I/O
A71	Type 6	LVDS_A0+	LVDS channel A differential signal pair 0	O LVDS
A72	Type 10	LVDS_A0-		
A73	Type 6	LVDS_A1+	LVDS channel A differential signal pair 1	O LVDS
A74	Type 10	LVDS_A1-		
A75	Type 6	LVDS_A2+	LVDS channel A differential signal pair 2	O LVDS
A76	Type 10	LVDS_A2-		
A78	Type 6	LVDS_A3+	LVDS channel A differential signal pair 3	O LVDS
A79	Type 10	LVDS_A3-		
A81	Type 6	LVDS_A_CK+	LVDS channel A differential clock pair	O LVDS
A82	Type 10	LVDS_A_CK-		
B71	Type 6	LVDS_B0+	LVDS channel B differential signal pair 0	O LVDS
B72		LVDS_B0-		
B73	Type 6	LVDS_B1+	LVDS channel B differential signal pair 1	O LVDS
B74		LVDS_B1-		
B75	Type 6	LVDS_B2+	LVDS channel B differential signal pair 2	O LVDS
B76		LVDS_B2-		
B77	Type 6	LVDS_B3+	LVDS channel B differential signal pair 3	O LVDS
B78		LVDS_B3-		
B81	Type 6	LVDS_B_CK+	LVDS channel B differential clock pair	O LVDS
B82		LVDS_B_CK-		
A77	Type 6 Type 10	LVDS_VDD_EN	LVDS flat panel power enable.	O 3.3V, CMOS
B79	Type 6 Type 10	LVDS_BKLT_EN	LVDS flat panel backlight enable high active signal	O 3.3V, CMOS
B83	Type 6 Type 10	LVDS_BKLT_CTRL	LVDS flat panel backlight brightness control	O 3.3V, CMOS
A83	Type 6 Type 10	LVDS_I2C_CK	DDC I2C clock signal used for flat panel detection and control.	O 3.3V, CMOS
A84	Type 6 Type 10	LVDS_I2C_DAT	DDC I2C data signal used for flat panel detection and control.	I/O 3.3V, OD CMOS

3.3.6.2 LVDS Reference Schematics

Figure 3-9 LVDS Reference Schematic



Note : TVS placement must be close to Connector for ESD Solution .

3.3.6.3 LVDS Layout Recommendations

Table 3-13: LVDS Trace Routing Guidelines

Parameter	Trace Routing
Max signal line length to the LVDS connector	8.75 inches
Carrier Board Signal length	6.75 inches
Differential Impedance	100 Ω +/-20% (Impedence may vary when different LVDS IC used)
Single-ended Impedance	55 Ω +/-15%
Trace width / differential pairs Spacing (intra-pair)	PCB stack-up dependent
Spacing between pair to pairs (inter-pair)	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 20mils
Spacing between differential pairs and low-speed non periodic signals	Min. 20mils
Length matching between differential pairs (intra-pair)	+/- 20mils
Length matching between clock and data pairs (inter-pair)	+/- 20mils
Length matching between data pairs	+/- 40mils
Spacing from edge of plane	+/- 40mils
Reference plane	Ground
Via Usage	Max. of 2 vias per line

3.3.7 Embedded DisplayPort

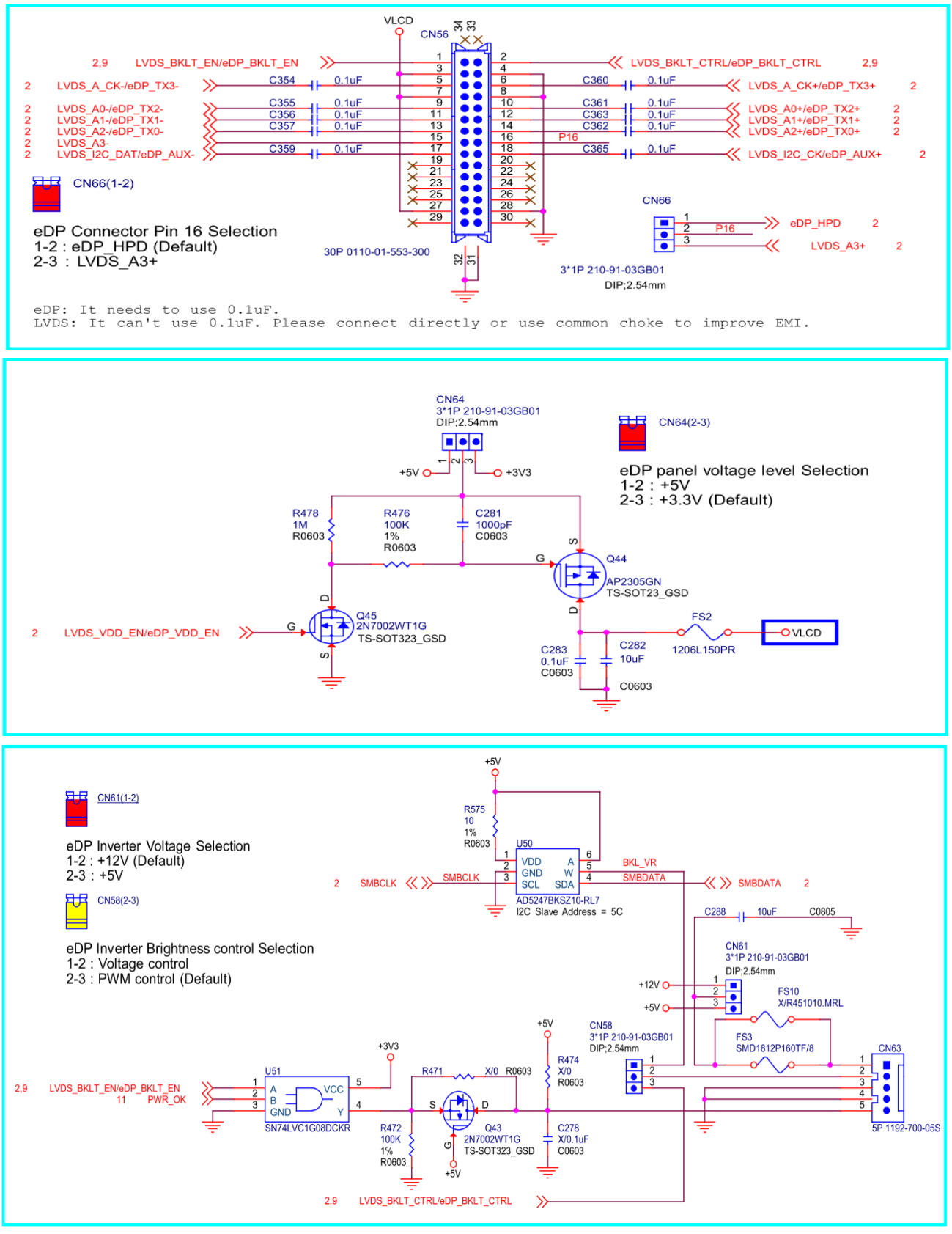
3.3.7.1 Signal Definitions

Table 3-14: Embedded DisplayPort Signal Definitions

Pin	Type	Signal	Description	I/O
A75	Type 6 Type 10	eDP_TX0+	eDP lane 0, TX +	O PCIe
A76	Type 6 Type 10	eDP_TX0-	eDP lane 0, TX -	O PCIe
A73	Type 6 Type 10	eDP_TX1+	eDP lane 1, TX +	O PCIe
A74	Type 6 Type 10	eDP_TX1-	eDP lane 1, TX -	O PCIe
A71	Type 6 Type 10	eDP_TX2+	eDP lane 2, TX +	O PCIe
A72	Type 6 Type 10	eDP_TX2-	eDP lane 2, TX -	O PCIe
A81	Type 6 Type 10	eDP_TX3+	eDP lane 3, TX +	O PCIe
A82	Type 6 Type 10	eDP_TX3-	eDP lane 3, TX -	O PCIe
A77	Type 6 Type 10	eDP_VDD_EN	eDP power enable	O CMOS
B79	Type 6 Type 10	eDP_BLKT_EN	eDP backlight enable	O CMOS
B83	Type 6 Type 10	eDP_BLKT_CTRL	EDP backlight brightness control	O CMOS
A83	Type 6 Type 10	eDP_AUX+	eDP auxiliary lane +	I/O PCIe
A84	Type 6 Type 10	eDP_AUX-	eDP auxiliary lane -	I/O PCIe
A87	Type 6 Type 10	eDP_HPD	Detection of Hot Plug / Unplug and notification of the link layer	I CMOS

3.3.7.2 Embedded DisplayPort Reference Schematics

Figure 3-10 eDP Reference Schematic



3.3.7.3 Embedded DisplayPort Layout Recommendations: BY PLATFORM LAYOUT GUIDE

3.3.8 VGA

The COM Express Specification defines an analog VGA RGB interface for all Module types.

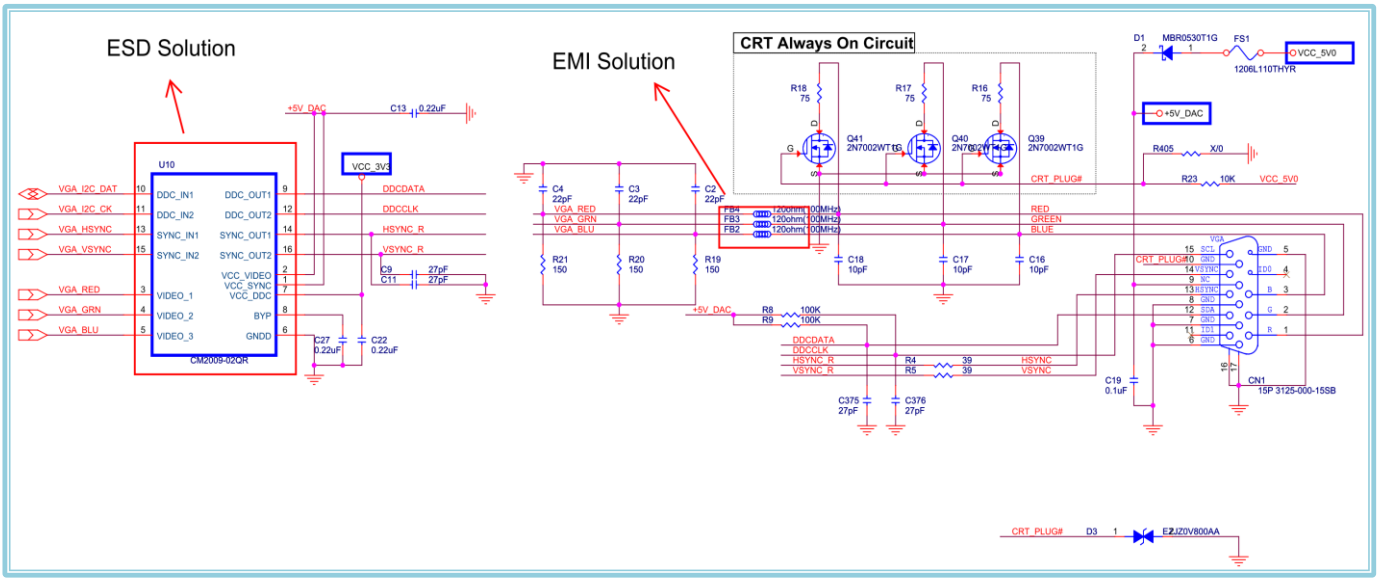
3.3.8.1 Signal Definitions

Table 3-15: VGA Signal Definitions

Pin	Type	Signal	Description	I/O
B89	Type 6	VGA_RED	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog
B91	Type 6	VGA_GRN	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog
B92	Type 6	VGA_BLU	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.	O Analog
B93	Type 6	VGA_HSYNC	Horizontal sync output to VGA monitor.	O 3.3V CMOS
B94	Type 6	VGA_VSYNC	Vertical sync output to VGA monitor.	O 3.3V CMOS
B95	Type 6	VGA_I2C_CK	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).	O 3.3V CMOS
B96	Type 6	VGA_I2C_DAT	DDC data line.	I/O 3.3V CMOS

3.3.8.2 VGA Reference Schematics

Figure 3-11 VGA Connector Reference Schematic



Note : CM2009 placement must be close to Connector for ESD Solution .

3.3.8.3 VGA Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.9 Digital Display

Module Types 6 and 10 use Digital Display Interfaces (DDI) to provide DisplayPort, HDMI/DVI, and SDVO interfaces. Type 10 Modules can contain a single DDI (DDI[0]) that can support DisplayPort, HDMI/DVI, and SDVO. Type 6 Modules can contain up to 3 DDIs (DDI[1:3]) of which DDI[1:3] can support DisplayPort, HDMI/DVI.

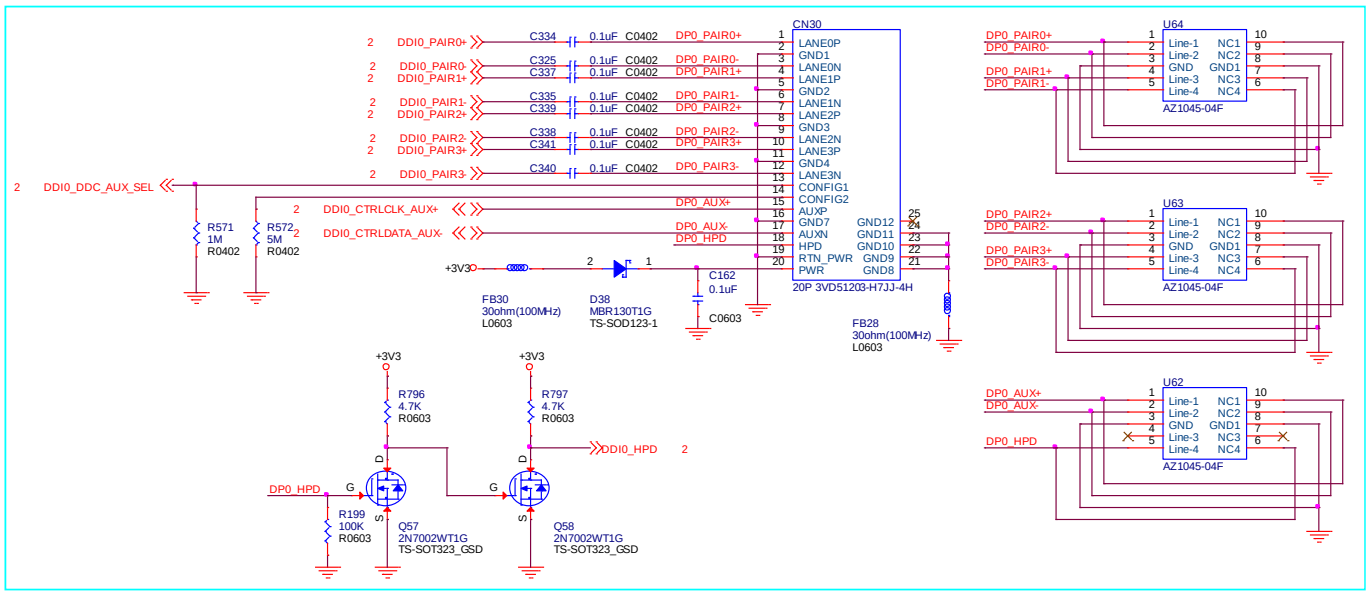
3.3.9.1 Signal Definitions

Table 3-16: Digital Display Signal Definitions

COM Express Pin Name	DDI0 Type 10	DDI1 Type 6	DDI2 Type 6	DDI3 Type 6	Function(DDIX) DisplayPort	Function (DDIX) HDMI / DVI
DDIX_PAIR0+	B71	D26	D39	C39	DPX_LANE0+	TMDSX_DATA2+
DDIX_PAIR0-	B72	D27	D40	C40	DPX_LANE0-	TMDSX_DATA2-
DDIX_PAIR1+	B73	D29	D42	C42	DPX_LANE1+	TMDSX_DATA1+
DDIX_PAIR1-	B74	D30	D43	C43	DPX_LANE1-	TMDSX_DATA1-
DDIX_PAIR2+	B75	D32	D46	C46	DPX_LANE2+	TMDSX_DATA0+
DDIX_PAIR2-	B76	D33	D47	C47	DPX_LANE2-	TMDSX_DATA0-
DDIX_PAIR3+	B81	D36	D49	C49	DPX_LANE3+	TMDSX_CLK+
DDIX_PAIR3-	B82	D37	D50	C50	DPX_LANE3-	TMDSX_CLK-
DDIX_HPD	B89	C24	D44	C44	DPX_HPD	HDMIX_HPD
DDIX_CTRLCLK_AUX+	B98	D15	C32	C36	DPX_AUX+	HDMIX_CTRLCLK
DDIX_CTRLDATA_AUX-	B99	D16	C33	C37	DPX_AUX-	HDMIX_CTRLDATA
DDIX_DDC_AUX_SEL	B95	D34	C34	C38		

3.3.9.2 Digital Display Reference Schematics

Figure 3-12 DP Connector Reference Schematic



Note: TVS placement must be close to Connector for ESD Solution.

3.3.9.3 Digital Display Layout Recommendations

Table 3-17: DisplayPort Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate	Max. 5.4 GBit/s
Carrier Board Signal length	3.2 inches
Differential Impedance	85 Ω +/-10% (Impedence may vary when different platform used)
Single-ended Impedance	50 Ω +/-15%
Trace width / differential pairs Spacing (intra-pair)	PCB stack-up dependent
Spacing between pair to pairs	Min. 15mils
Spacing between differential pairs and high-speed periodic signals	Min. 15mils
Spacing between differential pairs and low-speed non periodic signals	Min. 15mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Length matching between differential pairs (inter-pair)	Max 1 inch
Spacing from edge of plane	Min. 40mils
Via Usage	Max. 2
AC coupling capacitors	100nF

3.3.10 Digital Audio

The COM Express Specification allocates seven pins on the A-B connector to support digital AC'97 and HD interfaces to audio Codecs on the Carrier Board. The pins are available on all Module types. High-definition (HD) audio uses the same digital-signal interface as AC '97 audio. Codecs for AC '97 and HD Audio are different.

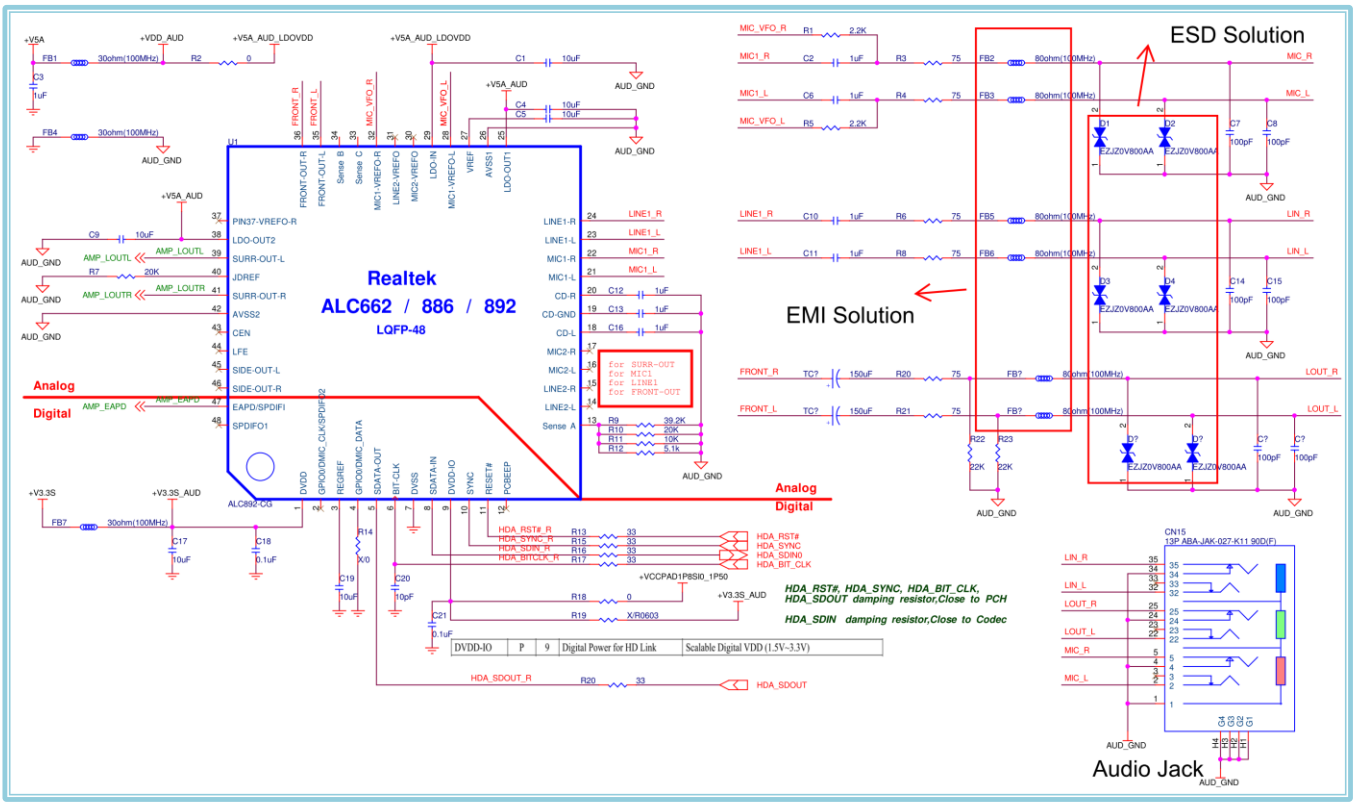
3.3.10.1 Signal Definitions

Table 3-18: Digital Audio Signal Definitions

Pin	Type	Signal	Description	I/O
A29	Type 6 Type 10	AC/HDA_SYNC	Serial Sample Rate Synchronization.	O 3.3V CMOS
A30	Type 6 Type 10	AC/HDA_RST#	CODEC Reset.	O 3.3V Suspend CMOS
A32	Type 6 Type 10	AC/HDA_BITCLK	24 MHz Serial Bit Clock for HDA CODEC.	O 3.3V CMOS
A33	Type 6 Type 10	AC/HDA_SDOUT	Audio Serial Data Output Stream.	O 3.3V CMOS
B28	Type 6 Type 10	AC/HDA_SDIN2	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS
B29	Type 6 Type 10	AC/HDA_SDIN1	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS
B30	Type 6 Type 10	AC/HDA_SDIN0	Audio Serial Data Input Stream from CODEC[0:2].	I 3.3V Suspend CMOS

3.3.10.2 Digital Audio Reference Schematics

Figure 3-13 Audio Jack Reference Schematic



Note : VDR placement must be close to Connector for ESD Solution .

3.3.10.3 Digital Audio Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.11 LPC

COM Express is designed to be a legacy free standard for embedded modules. It does not support legacy functionality on the Module, such as PS/2 keyboard/mouse, serial ports, and parallel ports. It provides an LPC interface that can be used to add peripheral devices to the Carrier Board design. AAEON can provide the available LPC IO schematic for customer's reference design.

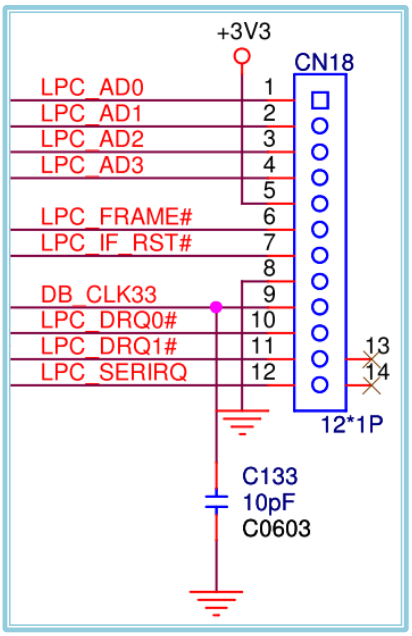
3.3.11.1 Signal Definitions

Table 3-19: LPC Signal Definitions

Pin	Type	Signal	Description	I/O
A50	Type 6,7 Type 10	LPC_SERIRQ	LPC serialized IRQ.	I/O 3.3V CMOS
B3	Type 6,7 Type 10	LPC_FRAME#	LPC frame indicates start of a new cycle or termination of a broken cycle.	O 3.3V CMOS
B4	Type 6,7 Type 10	LPC_AD0	LPC multiplexed command, address and data.	I/O 3.3V CMOS
B5		LPC_AD1		
B6		LPC_AD2		
B7		LPC_AD3		
B8	Type 6,7 Type 10	LPC_DRQ0#	LPC encoded DMA/Bus master request.	I 3.3V CMOS
B9		LPC_DRQ1#		
B10	Type 6,7 Type 10	LPC_CLK	LPC clock output 33MHz.	O 3.3V CMOS

3.3.11.2 LPC Reference Schematics

Figure 3-14 LPC Debug Connector Reference Schematic



3.3.11.3 LPC Layout Recommendations

Table 3-20: LPC Trace Routing Guidelines

Parameter	Trace Routing
Transfer Rate @ 33MHz	16 MBit/s
Carrier Board Max data and control signal length	15.0 inches
Carrier Board Max clock signal length	8.88 inches
Single-ended Impedance	55 Ω +/-15% (Impedence may vary when different platform used)
Trace width / Spacing between signals (inter-signal)	PCB stack-up dependent
Length matching between single ended / clock signals	Max. 200mils
Spacing from edge of plane	Min. 40mils
Reference plane	Ground
Via Usage	Try to minimize number of vias

3.3.12 SPI

The SPI interface is defined in this specification to service as an off-module option for BIOS storage. The SPI interface replaces the LPC Firmware Hub interface, which is now considered a legacy interface for firmware storage (LPC does continue to be used for SuperIO connectivity).

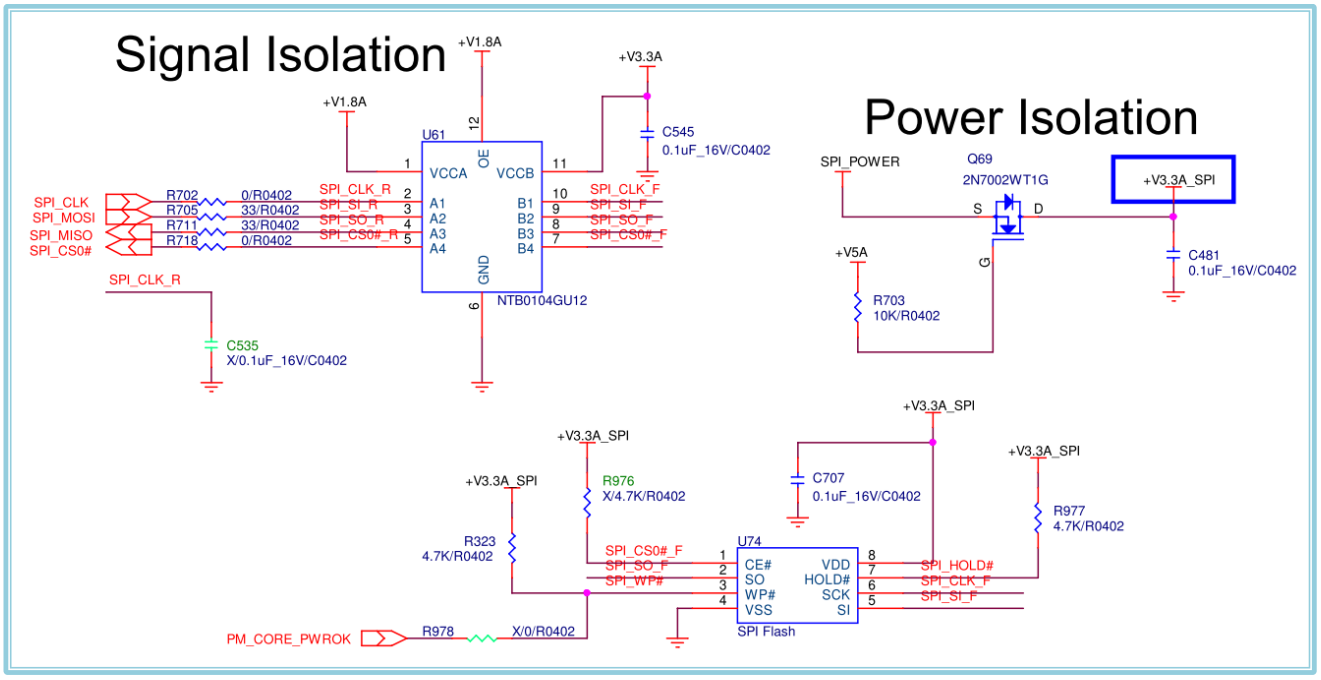
3.3.12.1 Signal Definitions

Table 3-21: SPI Signal Definitions

Pin	Type	Signal	Description	I/O
B97	Type 6,7 Type 10	SPI_CS#	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1	O CMOS – 3.3V Suspend
A92	Type 6,7 Type 10	SPI_MISO	Data in to Module from Carrier SPI	I CMOS – 3.3V Suspend
A95	Type 6,7 Type 10	SPI_MOSI	Data out from Module to Carrier SPI	O CMOS – 3.3V Suspend
A94	Type 6,7 Type 10	SPI_CLK	Clock from Module to Carrier SPI	O CMOS – 3.3V Suspend
A91	Type 6,7 Type 10	SPI_POWER	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier.	O – 3.3V Suspend
A34	Type 6,7 Type 10	BIOS_DIS0#	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals.	I CMOS
B88	Type 6,7 Type 10	BIOS_DIS1#	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low.	I CMOS

3.3.12.2 SPI Reference Schematics

Figure 3-15 SPI Connector Reference Schematic



Note: SPI Signals must be added isolation circuit(level shift or N MOSFET) for System protection.

3.3.12.3 SPI Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.13 I2C

The I2C (Inter-Integrated Circuit) bus is a two-wire serial bus originally defined by Philips. The bus is used for low-speed (up to 400kbps) communication between system ICs. The bus is often used to access small serial EEPROM memories and to set up IC registers. The COM Express Specification defines several I2C interfaces that are brought to the Module connector for use on the Carrier. Some of these interfaces are for very specific functions (VGA, LVDS, and DDIX), one interface is the SMBus used primarily for management and one other interface is a general purpose I2C interface. Since COM.0 Rev. 2.0 this interface should support multi-master operation. This capability will allow a carrier to read an optional module EEPROM before powering up the module.

3.3.13.1 Signal Definitions

Table 3-22: I2C Signal Definitions

Pin	Type	Signal	Description	I/O
B33	Type 6,7 Type 10	I2C_CK	General Purpose I2C Clock output	I/O OD CMOS
B34	Type 6,7 Type 10	I2C_DAT	General Purpose I2C data I/O line.	I/O OD CMOS

3.3.14 SMBus

The SMBus is primarily used as an interface to manage peripherals such as serial presence detect (SPD) on RAM, thermal sensors, PCI/PCIe devices, smart battery, etc. The devices that can connect to the SMBus can be located on the Module and Carrier. The SMBus is similar to I2C. I2C devices have the potential to lock up the data line while sending information and require a power cycle to clear the fault condition. SMBus devices contain a timeout to monitor for and correct this condition. Designers are urged to use SMBus devices when possible over standard I2C devices.

3.3.14.1 SMBus Signal Definitions

Table 3-23: SMBus Signal Definitions

Pin	Type	Signal	Description	I/O
B13	Type 6,7 Type 10	SMB_CK	System Management Bus bidirectional clock line	I/O OD CMOS
B14	Type 6,7 Type 10	SMB_DAT	System Management bidirectional data line.	I/O OD CMOS
B15	Type 6,7 Type 10	SMB_ALERT#	System Management Bus Alert	I CMOS

3.3.15 CANBUS

CAN bus is a vehicle bus standard designed to allow controllers and devices to communicate with each other without a host computer. CAN bus is a message-based protocol, designed specifically for automotive applications but now also used in other areas such as industrial automation and medical equipment.

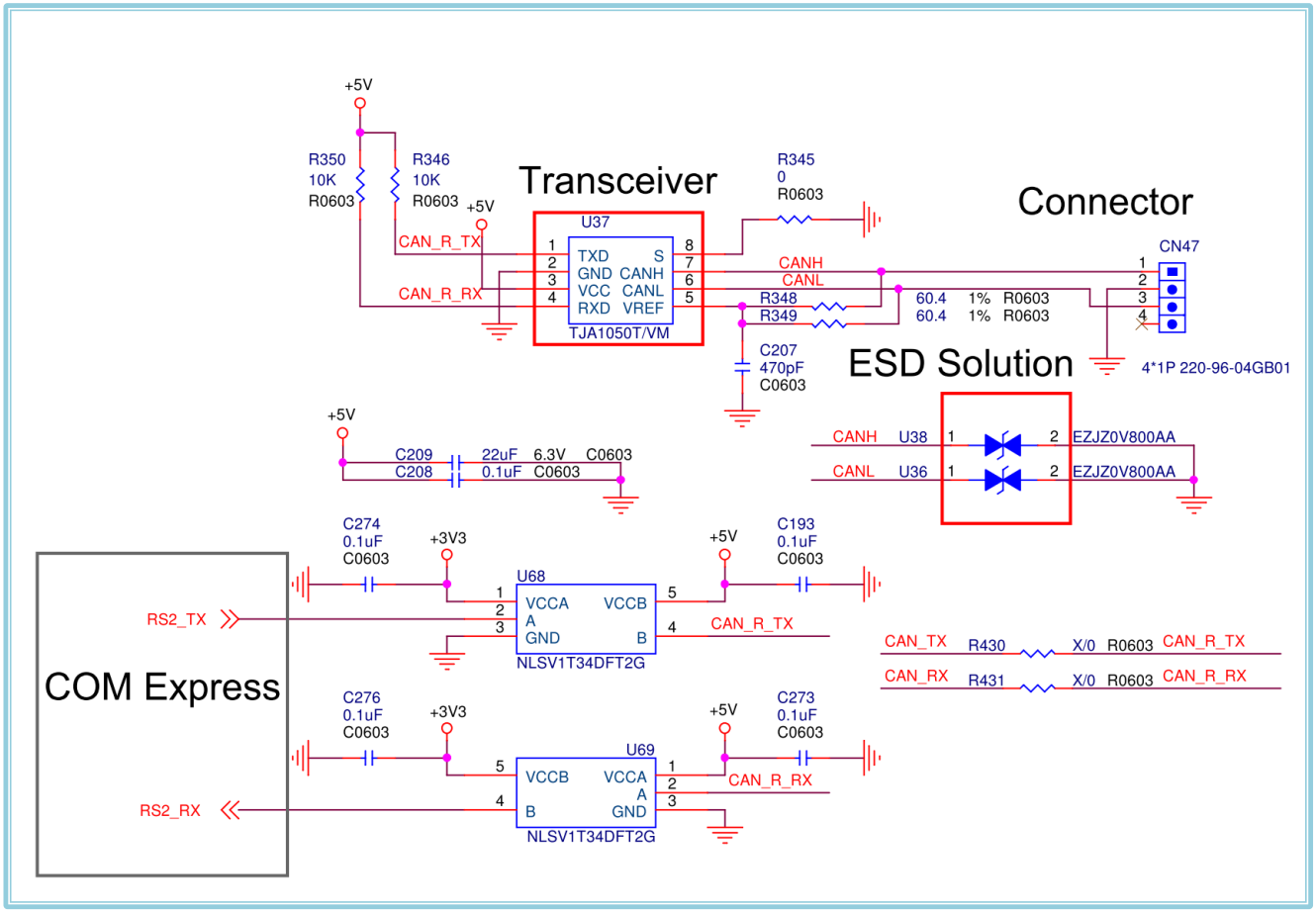
3.3.15.1 Signal Definitions

Table 3-24: CANBUS Signal Definitions

Pin	Type	Signal	Description	I/O
A101	Type 6,7 Type 10	SER1_TX	Transmit Line for CAN (can be shared with SER1 function)	O CMOS (protected)
A102	Type 6,7 Type 10	SER1_RX	Receive Line for CAN (can be shared with SER1 function)	I CMOS (protected)

3.3.15.2 CANBUS Reference Schematics

Figure 3-16 CANBUS Connector Reference Schematic



Note : VDR placement must be close to Connector for ESD Solution .

3.3.15.3 CANBUS Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.16 RTC Battery

The Real Time Clock (RTC) is responsible for maintaining the time and date even when the COM Express Module is not connected to a main power supply. Usually a +3V lithium battery cell is used to supply the internal RTC of the Module. The COM Express Specification defines an extra power pin 'VCC_RTC', which connects the RTC of the Module to the external battery. The specified input voltage range of the battery is defined between +2.0V and +3.0V. The signal 'VCC_RTC' can be found on the Module's connector row A pin A47.

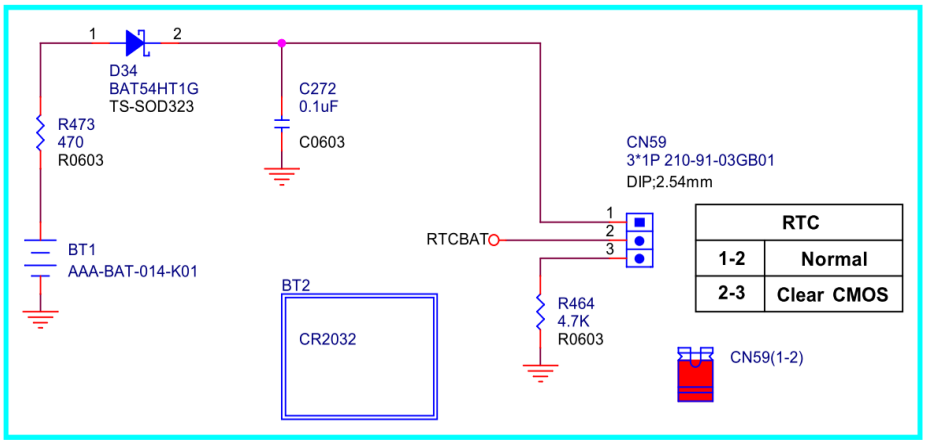
3.3.16.1 Signal Definitions

Table 3-25: RTC Battery Signal Definitions

Pin	Type	Signal	Description	I/O
A47	Type 6,7 Type 10	VCC_RTC	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS

3.3.16.2 RTC Battery Reference Schematics

Figure 3-17 RTC Connector Reference Schematic



3.3.16.3 RTC Battery Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.17 DIO

General Purpose Input / Output (GPIO)

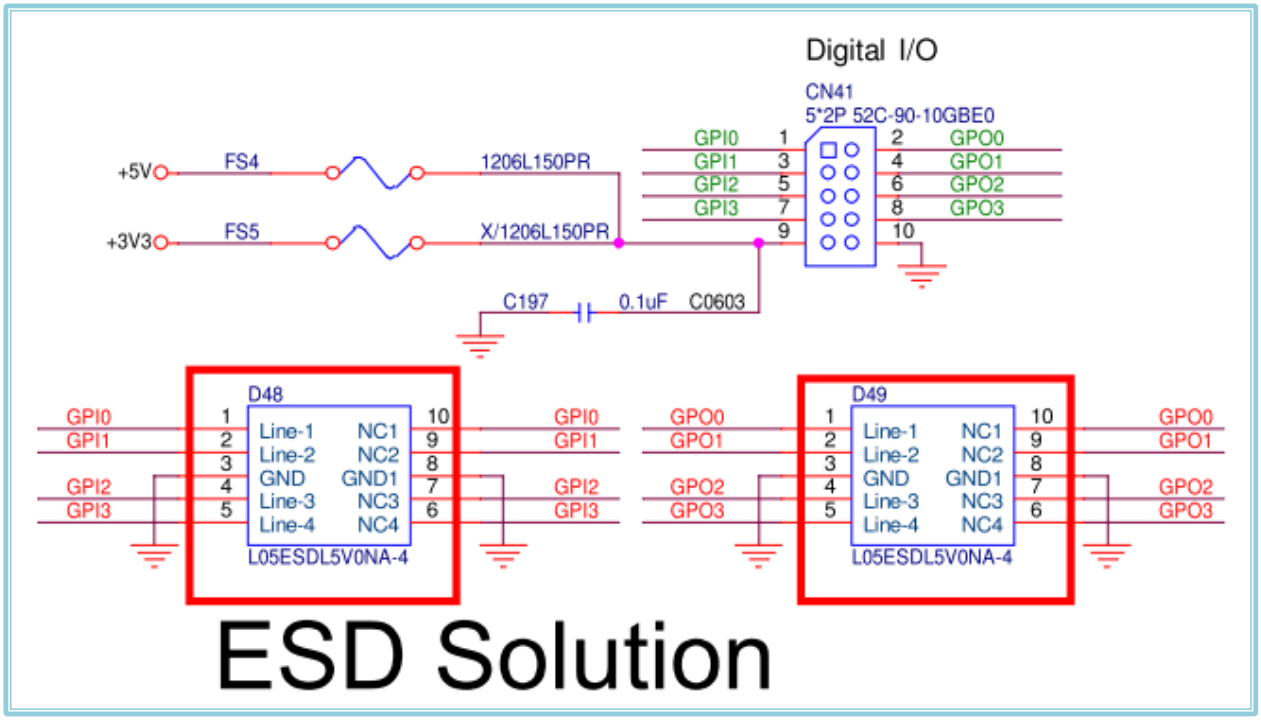
3.3.17.1 Signal Definitions

Table 3-26: DIO Signal Definitions

Pin	Type	Signal	Description	I/O
A54	Type 6,7 Type 10	GPI0	General purpose input pins. Pulled high internally on the Module.	I 3.3V CMOS
A63		GPI1		
A67		GPI2		
A85		GPI3		
A93	Type 6,7 Type 10	GPO0	General purpose output pins. Upon a hardware reset, these outputs should be low.	O 3.3V CMOS
B54		GPO1		
B57		GPO2		
B63		GPO3		

3.3.17.2 DIO Reference Schematics

Figure 3-18 DIO Connector Reference Schematic



Note : (1) TVS placement must be close to Connector for ESD Solution .

(2) SDIO and DIO share the GPIO pin .

3.3.17.3 DIO Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.18 SDIO

SD Card support was added in COM.0 Rev. 2.0 as an alternative use for the GPIO pins.

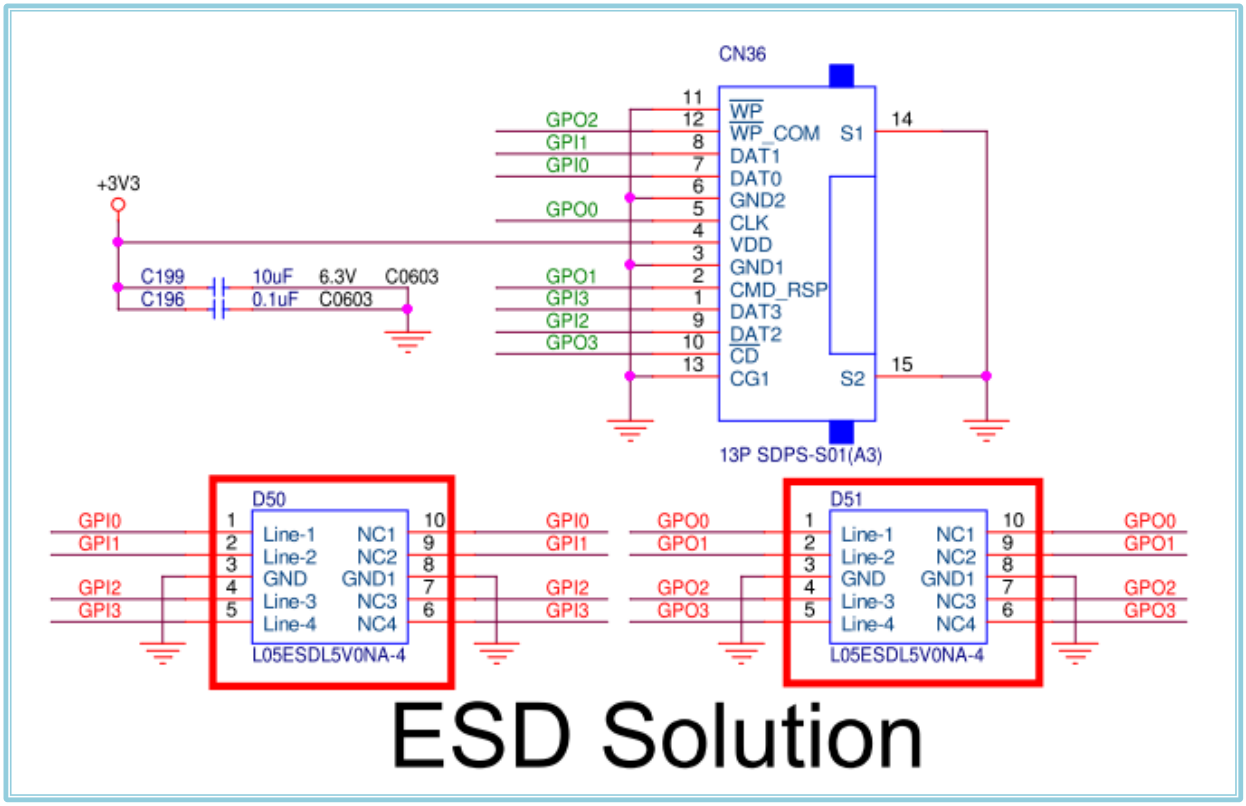
3.3.18.1 Signal Definitions

Table 3-27: SDIO Signal Definitions

Pin	Type	COM Express Signal	SD Card Interface Signals
A54	Type 6,7 Type 10	GPI0	SD_DATA0
A63		GPI1	SD_DATA1
A67		GPI2	SD_DATA2
A85		GPI3	SD_DATA3
A93	Type 6,7 Type 10	GPO0	SD_CLK
B54		GPO1	SD_CMD
B57		GPO2	SD_WP
B63		GPO3	SD_CD#

3.3.18.2 SDIO Reference Schematics

Figure 3-19 SDIO Connector Reference Schematic



Note : (1) TVS placement must be close to Connector for ESD Solution .

(2) SDIO and DIO share the GPIO pin .

3.3.18.3 SDIO Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.19 Serial Interface

General Purpose Serial Interface ,Since Revision 2.0 of the COM Express specification two optional serial ports are available on Type 10 and Type 6 COM Express Modules uses pins on the A-B connector.

3.3.19.1 Signal Definitions

Table 3-28: Serial Interface Signal Definitions

Pin	Type	Signal	Description	I/O
A98	Type 6,7 Type 10	SER0_TX	Transmit Line for Serial Port 0	O CMOS (protected)
A99	Type 6,7 Type 10	SER0_RX	Receive Line for Serial Port 0	I CMOS (protected)
A101	Type 6,7 Type 10	SER1_TX	Transmit Line for Serial Port 1 (can be shared with CAN function)	O CMOS (protected)
A102	Type 6,7 Type 10	SER1_RX	Receive Line for Serial Port 1 (can be shared with CAN function)	I CMOS (protected)

3.3.19.2 Serial Interface Reference Schematics : BY PLATFORM LAYOUT GUIDE

3.3.19.3 Serial Interface Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.20 Power Management Signals

3.3.20.1 Signal Definitions

Table 3-29: Power Management Signal Definitions

Pin	Type	Signal	Description	I/O
B12	Type 6,7 Type 10	PWRBTN#	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.	I 3.3V Suspend CMOS
B49	Type 6,7 Type 10	SYS_RESET#	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	I 3.3V Suspend CMOS
B50	Type 6,7 Type 10	CB_RESET#	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board.	O 3.3V Suspend CMOS
B24	Type 6,7 Type 10	PWR_OK	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation.	I 3.3V CMOS
B18	Type 6,7 Type 10	SUS_STAT#	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode.	O 3.3V Suspend CMOS
A15	Type 6,7 Type 10	SUS_S3#	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).	O 3.3V Suspend CMOS
A18	Type 6,7 Type 10	SUS_S4#	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk).	O 3.3V Suspend CMOS
A24	Type 6,7 Type 10	SUS_S5#	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).	O 3.3V Suspend CMOS
B66	Type 6,7 Type 10	WAKE0#	PCI Express wake-up event signal.	I 3.3V Suspend CMOS
B67	Type 6,7 Type 10	WAKE1#	General purpose wake-up signal.	I 3.3V Suspend CMOS
A27	Type 6,7 Type 10	BATLOW#	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low.	I 3.3V Suspend CMOS

3.3.20.2 Power Management Reference Schematics

Figure 3-20 PWRBTN# Reference Schematic

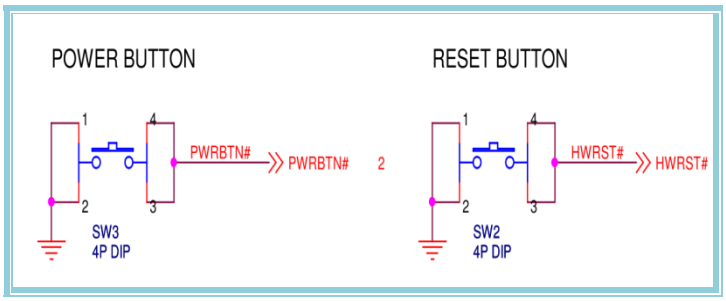


Figure 3-21 CB_RESET# Reference Schematic

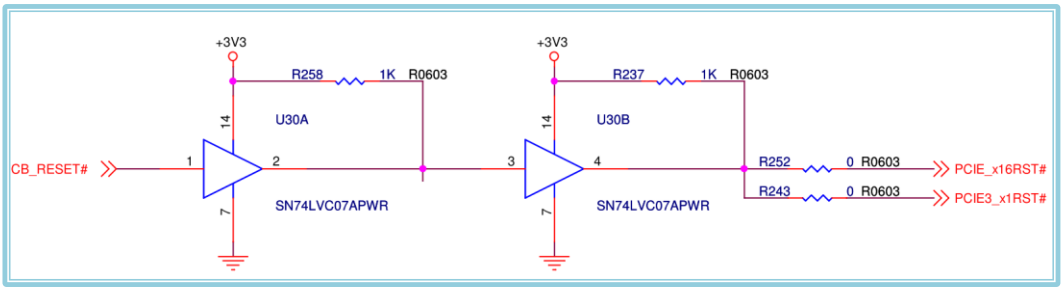
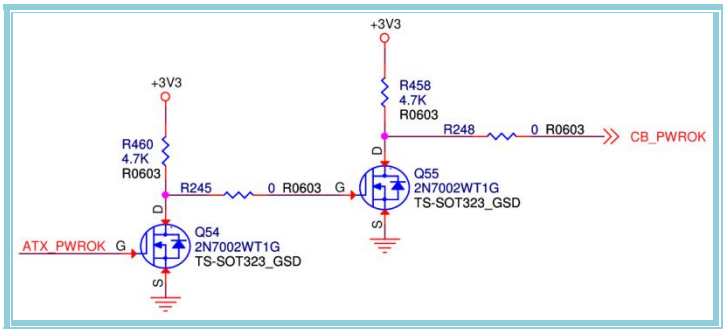


Figure 3-22 PWR_OK Reference Schematic



3.3.20.3 Power Management Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.21 FAN Connector

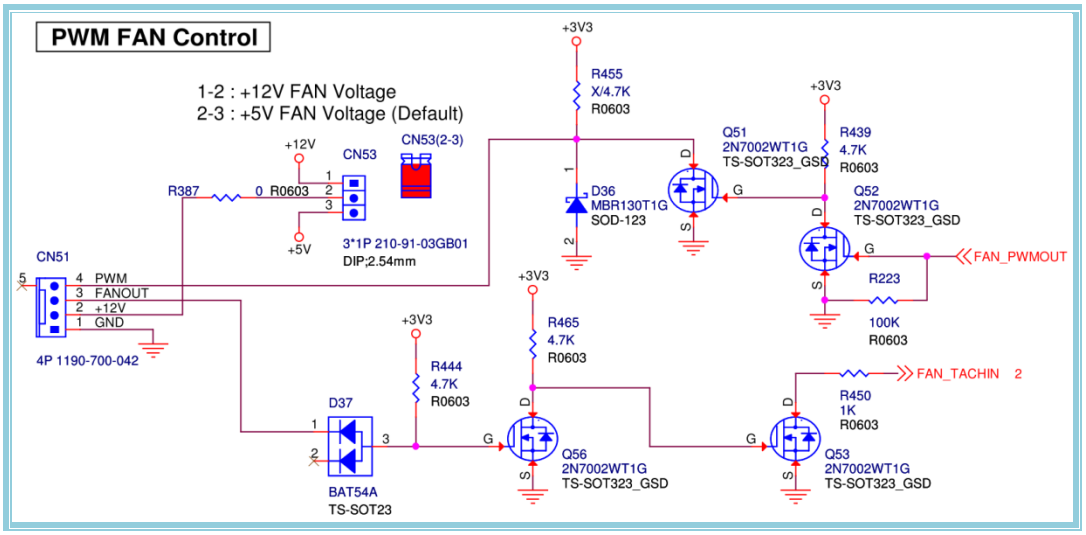
3.3.21.1 Signal Definitions

Table 3-30: FAN Connector Signal Definitions

Pin	Type	Signal	Description	I/O
B101	Type 6,7 Type 10	FAN_PWMOUT	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	O 3.3V CMOS OD
B102	Type 6,7 Type 10	FAN_TACHIN	Fan tachometer input for a fan with a two pulse output.	I 3.3V CMOS OD

3.3.21.2 FAN Connector Reference Schematics

Figure 3-23 FAN Connector Reference Schematics



3.3.21.3 FAN Connector Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.22 Miscellaneous Signals

3.3.22.1 Signal Definitions

Table 3-31: Miscellaneous Signals Definitions

Pin	Type	Signal	Description	I/O
C54 C57 D57	Type 6,7	TYPE0# TYPE1# TYPE2#	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the Module. The pins are tied on the Module to either ground (GND) or are no-connects (NC). For Pin-out Type 1 and Type 10, these pins are not present (X). **TYPE0# TYPE1# TYPE2#** **GND NC NC Pin-out Type 6** The Carrier Board should implement combinatorial logic that monitors the Module TYPE pins and keeps power off (e.g. deactivates the ATX_ON signal for an ATX power supply) if an incompatible Module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.	O 5V PDS
A97	Type 6,7 Type 10	TYPE10#	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed. **TYPE10#** **NC Pin-out R2.0** **PD Pin-out Type 10 pull down to ground with 47k** **12V Pin-out R1.0**	
B32	Type 6,7 Type 10	SPKR	Output used to control an external FET or a logic gate to drive an external PC speaker.	O 3.3V CMOS
B27	Type 6,7 Type 10	WDT	Output indicating that a watchdog time-out event has occurred.	O 3.3V CMOS
A103	Type 6,7 Type 10	LID#	LID switch. Low active signal used by the ACPI operating system for a LID switch.	I 3.3V CMOS OD
B103	Type 6,7 Type 10	SLEEP#	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	I 3.3V CMOS OD
A96	Type 6,7 Type 10	TPM_PP	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	I 3.3V CMOS

3.3.22.2 Miscellaneous Signals Schematics

Figure 3-24 LID# and SLEEP# Reference Schematic

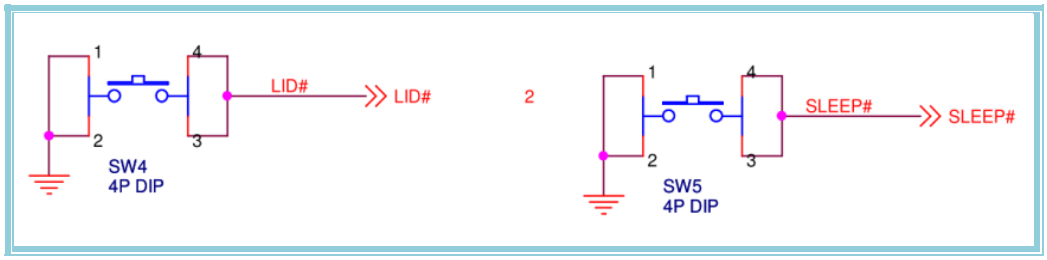


Figure 3-25 WDT Reference Schematic

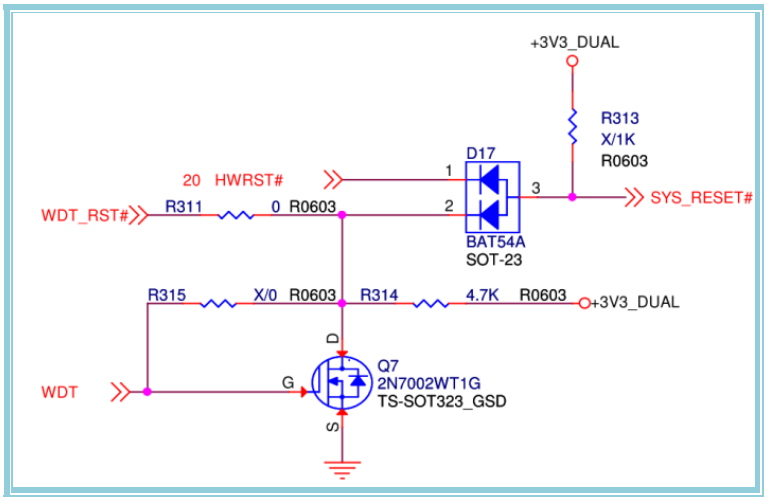
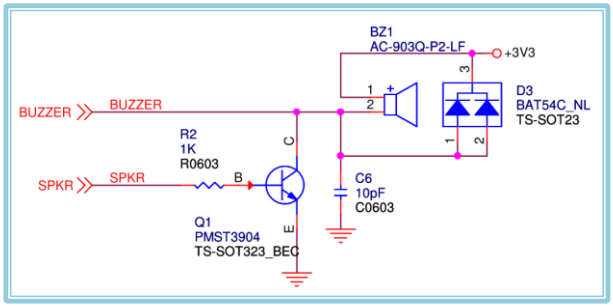


Figure 3-26 SPKR Reference Schematic



3.3.22.3 Miscellaneous Signals Layout Recommendations : BY PLATFORM LAYOUT GUIDE

3.3.23 10G Interface

10GBASE-KR support was added to COM Express with revision 3.0 of the specification.

Type 7 supports up to four 10GBASE-KR interfaces. The 10G MAC is located on the Module and the PHY is located on the Carrier. 10GBASE-KR uses a single transmit and a single receive ac coupled differential pair for data and a sideband bus for the PHY control and configuration. COM Express supports both MDIO and I2C control interfaces for the PHY.

The PHY control interfaces are grouped into pairs. 10G Ports 0 and 1 share a common PHY control interface and 10G ports 2 and 3 share a common PHY control interface. The PHY interface selection is made using the 10G_PHY_CAP_01 and 10G_PHY_CAP_23 pins. The Carrier design can select the PHY that is appropriate for the design. The Module designer should design the module in such a way that it can provide the PHY interface that is selected regardless of the capabilities of the silicon used on the Module. Appropriate level shifters shall be used.

A two wire I2C bus (designated 10G_LED_SDA and 10G_LED_SCL) is defined to serialize the outbound (Module to Carrier) MAC LED and PHY strapping signals, conserving COM Express pins. The Carrier should use a PCA9539 or compatible I2C I/O expander. The Carrier PCA9539 shall be mapped to I2C address 1110 100x (x=R/W bit). Table 14 below defines the port pin mapping for the I/O expander.

There are two pairs of PHY strapping signals defined. The first pair is designated as 10G_PHY_CAP_01 and 10G_PHY_CAP_23. These are actual COM Express pins. They are inputs to the COM Express Module. The Carrier may either tie these lines to GND or leave them NC on the Carrier. If 10G_PHY_CAP_01 is tied low on the Carrier, this indicates to the Module that the PHY on the Carrier for 10G interfaces 0 and 1 can be configured by either I2C or by MDIO. If the Carrier leaves the line NC, then this indicates to the Module that the Carrier PHY can only be configured by MDIO. Similarly for strap signal 10G_PHY_CAP_23 and 10G interfaces 2 and 3.

The second pair of PHY strapping signals are outputs from the Module, serialized onto the 10G_LED_Sxx I2C bus. They are desterilized on the Carrier I/O expander and may used to set Carrier PHY strapping pins to set the desired Carrier PHY configuration mode, if the PHY is capable of multiple configuration modes.

This arrangement with a pair of input straps (telling the Module what configuration modes are possible on the Carrier PHY) and a pair of serialized output straps (telling the Carrier PHY what configuration mode to use) allow Module designs that can use a variety of PHYs. In particular, Intel Broadwell DE Modules that can be used with either Intel "Coppervale" PHYs or with Inphy / Cortina PHYs can be realized.

3.3.23.1 Signal Definitions

Table 3-32: 10G Interface Signal Definitions

Pin	Type	Signal	Description	I/O
D49	Type 7	10G_KR_TX0+	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR
D50		10G_KR_TX0-		
C49	Type 7	10G_KR_RX0+	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR
C50		10G_KR_RX0-		
D42	Type 7	10G_KR_TX1+	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR
D43		10G_KR_TX1-		
C42	Type 7	10G_KR_RX1+	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR
C43		10G_KR_RX1-		
D29	Type 7	10G_KR_TX2+	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR
D30		10G_KR_TX2-		
C29	Type 7	10G_KR_RX2+	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board: N/C if not used.N/C if not used.	I KR
C30		10G_KR_RX2-		
D26	Type 7	10G_KR_TX3+	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR
D27		10G_KR_TX3-		
C26	Type 7	10G_KR_RX3+	10GBASE-KR port, receive input differential pairs. Module has integrated AC Coupling Capacitor. Carrier board:	I KR
C27		10G_KR_RX3-		

			N/C if not used.N/C if not used.	
D49 D50	Type 7	10G_KR_TX0+ 10G_KR_TX0-	10GBASE-KR port, transmit output differential pairs. Carrier board: Device - Connect AC Coupling cap 0.1uF near PHY. N/C if not used.	O KR
D46	Type 7	10G_PHY_MDIO_SDA0	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
C46	Type 7	10G_PHY_MDIO_SCL0	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
D45	Type 7	10G_PHY_MDIO_SDA1	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C data signal, of the 2-wire	I/O OD

			management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	CMOS 3.3V Suspend / 3.3V
C45	Type 7	10G_PHY_MDIO_SCL1	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
D16	Type 7	10G_PHY_MDIO_SDA2	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
C16	Type 7	10G_PHY_MDIO_SCL2	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C Clock signal, of the 2-wire	I/O OD

			management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	CMOS 3.3V Suspend / 3.3V
D15	Type 7	10G_PHY_MDIO_SDA3	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C data signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
C15	Type 7	10G_PHY_MDIO_SCL3	MDIO Mode: Management Data I/O interface mode data signal for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	OC MOS 3.3V Suspend / 3.3V
			I2C Mode: I2C Clock signal, of the 2-wire management interface used for serial data transfers between the MAC and an external PHY. Carrier board: Device-Connect to PHY circuit. N/C if not used.	I/O OD CMOS 3.3V Suspend / 3.3V
D35	Type 7	10G_PHY_CAP_01	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on	I CMOS 3.3V Suspend / 3.3V

			this input. The actual protocol used is indicated over the dedicated I2C interface (see Table 13) Carrier board:	
D34	Type 7	10G_PHY_CAP_23	PHY mode capability pin: Indicates if the PHY for 10G lanes 0 and 1 is capable of configuration by I2C. High indicates MDIO-only configuration, and low indicates configuration capability via I2C or MDIO. The actual protocol used for PHY configuration is determined by the module, in part based on this input. The actual protocol used is indicated over the dedicated I2C interface (see Table 13) Carrier board:	I CMOS 3.3V Suspend / 3.3V
C39	Type 7	10G_SFP_SDA0	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
D39	Type 7	10G_SFP_SCL0	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
C38	Type 7	10G_SFP_SDA1	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
D38	Type 7	10G_SFP_SCL1	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
C33	Type 7	10G_SFP_SDA2	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module.	I/O OD CMOS 3.3V Suspend

			Carrier board:	/ 3.3V
D33	Type 7	10G_SFP_SCL2	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
C32	Type 7	10G_SFP_SDA3	I2C data signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
D32	Type 7	10G_SFP_SCL3	I2C clock signal of the 2-wire management interface used by the 10GbE controller to access the management registers of an external Optical SFP Module. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
C37	Type 7	10G_LED_SCL	I2C Clock of the 2-wire interface that transfers LED and strap signals for I2C or MDIO operation of optical PHYs. Carrier board:	I/O OD CMOS 3.3V Suspend / 3.3V
C35	Type 7	10G_PHY_RST_01	Output signal that resets an optical PHY on port 0 and port1 (with copper PHY this signal is not used). Carrier board:	O CMOS 3.3V Suspend / 3.3V
C34	Type 7	10G_PHY_RST_23	Output signal that resets an optical PHY on port 0 and port3 (with copper PHY this signal is not used). Carrier board:	O CMOS 3.3V Suspend / 3.3V
C47	Type 7	10G_INT0	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V
D47	Type 7	10G_INT1	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V
C24	Type 7	10G_INT2	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller.	I CMOS 3.3V

			Carrier board:	Suspend / 3.3V
D24	Type 7	10G_INT3	Interrupt pin from copper PHY or optical SFP Module to the 10GbE controller. Carrier board:	I CMOS 3.3V Suspend / 3.3V
C40	Type 7	10G_SDP00	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V
D40	Type 7	10G_SDP01	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V
C17	Type 7	10G_SDP02	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V
D17	Type 7	10G_SDP03	Software-Definable Pins. Can also be used for IEEE1588 support such as a 1pps signal. See section 2.6.2 for details.	I/O CMOS 3.3V Suspend / 3.3V
C36	Type 7	10G_LED_SDA	I2C Data of the 2-wire interface that transfers LED signals and PHY straps for I2C or MDIO operation of optical PHYs.Refer to the details in table 14 'I2C Data Mapping to Carrier Board based PCA9539 I/O expander'	I/O OD CMOS 3.3V Suspend / 3.3V

3.3.23.2 10G Interface Reference Schematics : BY PLATFORM LAYOUT GUIDE

Figure 3-27 10G Interface Reference Schematic-1

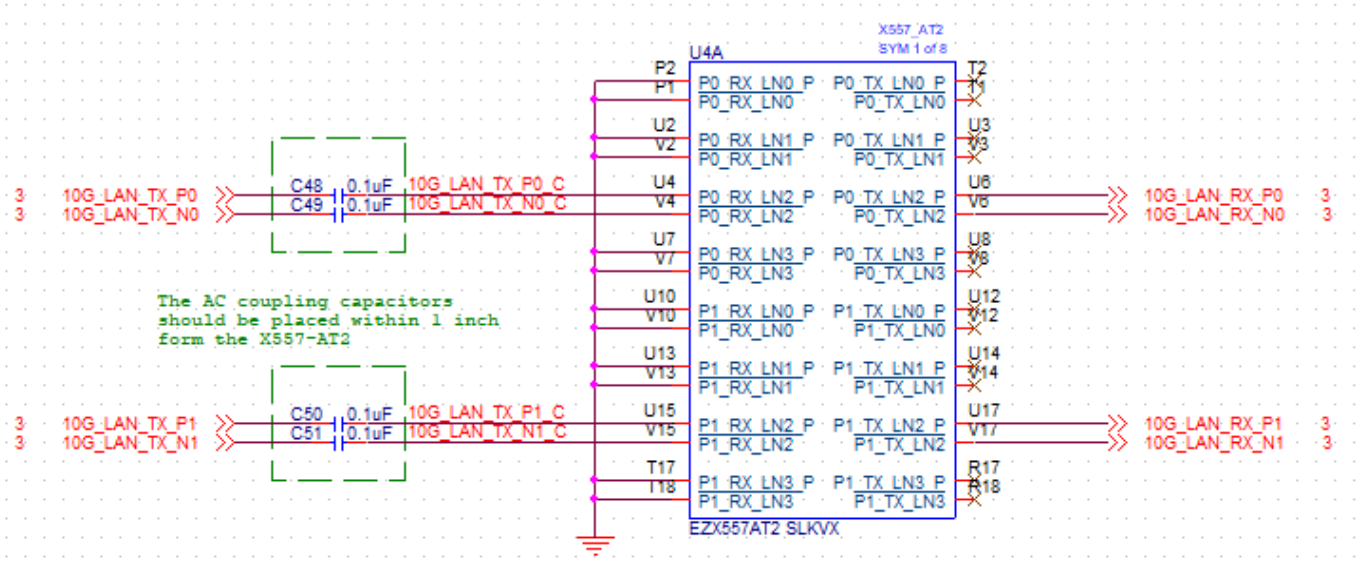


Figure 3-28 10G Interface Reference Schematic-2

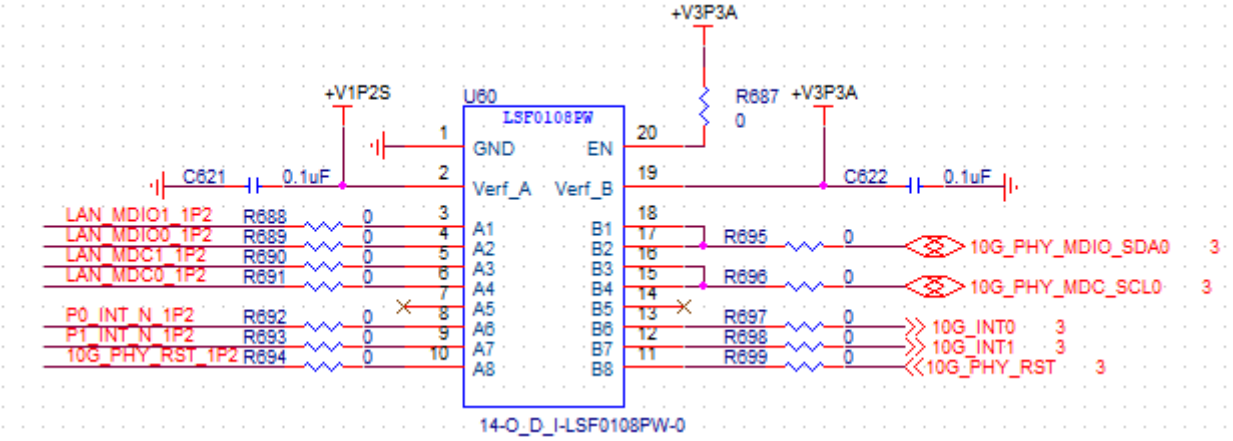


Figure 3-29 10G Interface Reference Schematic-3

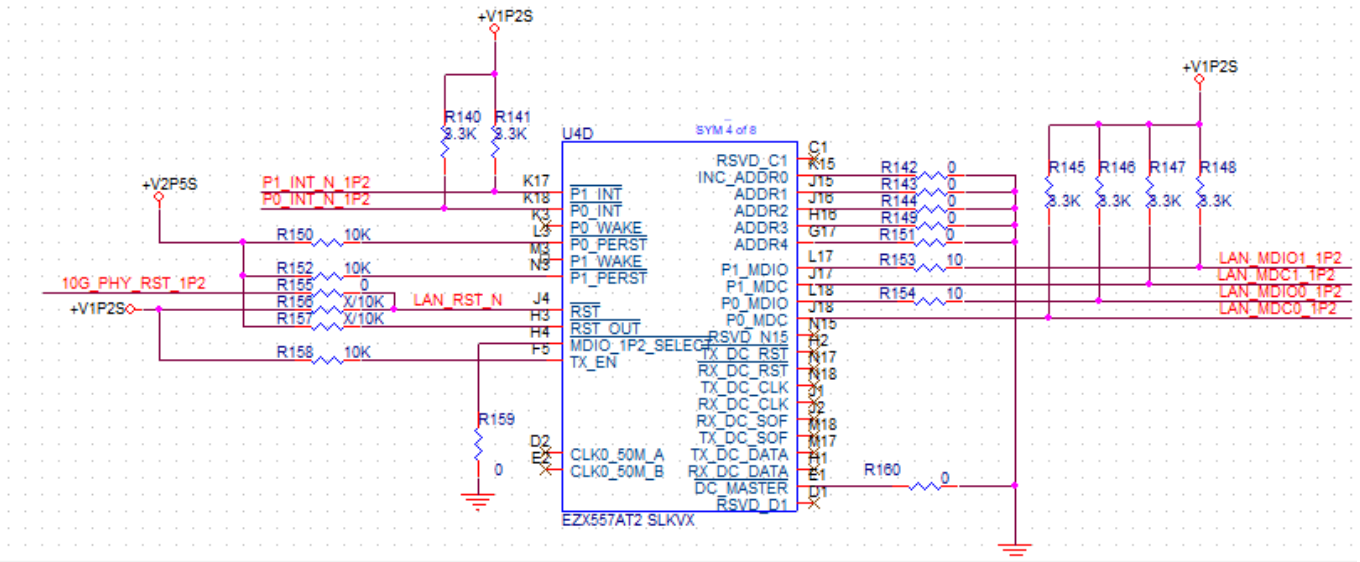
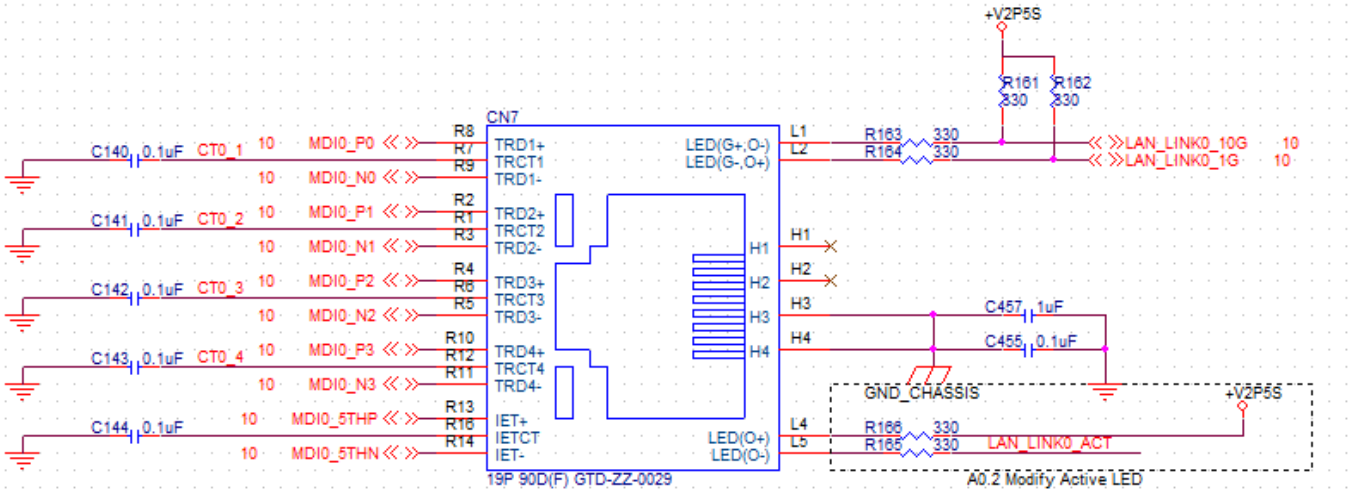


Figure 3-30 10G Interface Reference Schematic-4



3.3.23.3 10G Interface Layout Recommendations : BY PLATFORM LAYOUT GUIDE

Table 3-33: 10G Interface Layout Recommendations

Parameter	10GB LAN KR
Symbol Rate	10.0 Gb/s
Carrier Board Signal length	16.0 inches
Differential impedance	100 Ω +/-15% (Impedence may vary when different platform used)
Single-ended Impedance	50 Ω +/-15%
Trace width / Spacing between differential pairs	PCB stack-up dependent
Spacing between RX and TX (inter-pair) / differential pairs and low-speed non periodic signals	Min. 20mils
Spacing between differential pairs and high-speed periodic signals	Min. 50mils
Length matching between differential pairs (intra-pair)	Max. 5mils
Reference plane	GND referenced preferred
Length matching between RX and TX pairs (inter-pair)	No strict electrical requirements.Keep difference within a 3.0 inch delta to minimize latency.
Via Usage	Max. 2 vias per TX trace Max. 2 vias per RX trace
AC coupling capacitors	Capacitor type: X7R, 100nF +/- 10%, 16V, shape 0402.

3.3.24 NCSI Interface

The NC-SI ('Network Controller Sideband Interface') is an electrical interface and protocol defined by the Distributed Management Task Force (DMTF), which enables the connection of a BMC (Baseboard Management Controller) to enable out-of-band remote manageability. If implemented, the NC-SI shall be assigned to the GBE0 interface. NC-SI architecture also enables multiple endpoints to be connected to the same management controller.

In this configuration, the bus arbitration can also be implemented by hardware using a token ring configuration. The NCSI_ARB_IN pin of one controller must be connected to the NCSI_ARB_OUT of another controller to form a ring configuration. A maximum of four network controllers can be connected in this manner and all controllers sharing the same NC-SI interface pins must support this feature in order to use hardware-based arbitration. NCSI_ARB_IN and NCSI_ARB_OUT are to be left unconnected on the Carrier if there is no Carrier network controller.

3.3.24.1 Signal Definitions

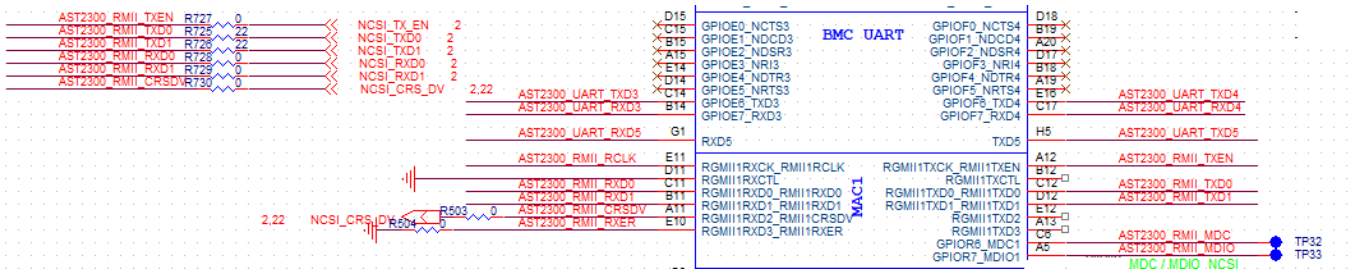
Table 3-34: NCSI Interface Signal Definitions

Pin	Type	Signal	Description	I/O
B89	Type 7	NCSI_RX_ER	NC-SI Receive error.	O COM 3.3V Suspend / 3.3V
B91	Type 7	NCSI_CLK_IN	NC-SI Clock reference for receive, transmit, and control interface.	I COM 3.3V Suspend / 3.3V
B92	Type 7	NCSI_RXD1	NC-SI Receive Data (from NC to BMC).	O COM 3.3V Suspend / 3.3V
B93	Type 7	NCSI_RXD0	NC-SI Receive Data (from NC to BMC).	O COM 3.3V Suspend / 3.3V
B94	Type 7	NCSI_CRS_DV	NC-SI Carrier Sense/Receive Data Valid to MC, indicating that t	O COM 3.3V Suspend / 3.3V
B95	Type 7	NCSI_TXD1	NC-SI Transmit Data (from BMC to NC).	I COM 3.3V Suspend / 3.3V
B96	Type 7	NCSI_TXD0	NC-SI Transmit Data (from BMC to NC).	I COM 3.3V Suspend / 3.3V
B98	Type 7	NCSI_ARB_IN	NC-SI hardware arbitration input. N/C if not used.	I COM 3.3V Suspend / 3.3V

B99	Type 7	NCSI_ARB_OUT	NC-SI hardware arbitration output. N/C if not used.	O COM 3.3V Suspend / 3.3V
A84	Type 7	NCSI_TX_EN	NC-SI Transmit enable.	I COM 3.3V Suspend / 3.3V

3.3.24.2 NCSI Interface Reference Schematics : BY PLATFORM LAYOUT GUIDE

Figure 3-31 NCSI Interface Reference Schematic



3.3.24.3 NCSI Interface Layout Recommendations : BY PLATFORM LAYOUT GUIDE

Table 3-35: NCSI Trace Routing Guidelines

Parameter	Trace Routing
Carrier Board Max data and control signal length	8.5 inches
Nominal Trace Space within LPC Signal Group	3H
Single-ended Impedance	50 Ω +/-15% (Impedence may vary when different platform used)
Trace width / Spacing between signals (inter-signal)	PCB stack-up dependent
Reference plane	Ground
Via Usage	Try to minimize number of vias

4. Power and Reset

4.1 ATX Power Sequence for +12 VDC and +5 VDC , +3.3 VDC

The +12 VDC and +5 VDC output levels must be equal to or greater than the +3.3 VDC output at all times during power-up and normal operation. The time between the +12 VDC or +5 VDC output reaching its minimum in-regulation level and +3.3 VDC reaching its minimum in-regulation level must be ≤ 20 ms.

(Refer : ATX12V Power Supply Design Guide_ Version 2.2)

Figure 4-1 ATX Power Supply Timing

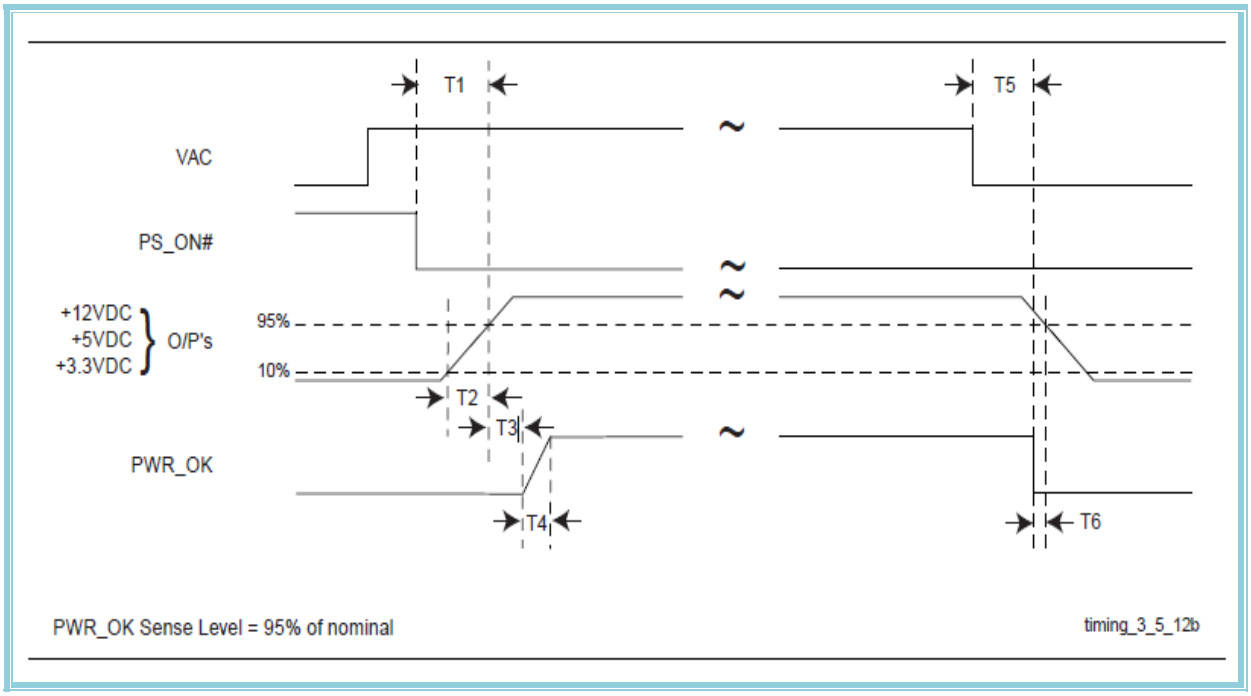


Table 4-1: ATX Power Signals Timing

Signal Type	Timing
Power-on Time	T1 < 500 ms
Rise time	0.1 ms ≤ T2 ≤ 20 ms
PWR_OK delay	100 ms < T3 < 500 ms
PWR_OK rise time	T4 ≤ 10 ms
AC loss to PWR_OK hold-up time	T5 ≥ 16 ms
Power-down warning	T6 ≥ 1 ms

4.2 COM Express ATX vs AT Supplies

ATX power supplies are in common use in contemporary PCs. ATX supplies have two sets of power rails: a set for normal operation (12V, 5V, 3.3V and -12V) and a separate 5V Suspend rail. The 5V Suspend rail is present whenever the ATX supply has AC input power. The other rails are on only when a control signal from the PC hardware known as PS_ON# is held low by the motherboard, allowing software control of the power supply. The PC motherboard may implement several mechanisms for controlling the AC power, including a push button switch that switches a low voltage logic signal rather than the AC main power. Other options may be implemented, including the capability to turn on the main power on events such as a keyboard press, mouse activity, etc.

AT power supplies do not have a Suspend rail and do not allow software control of the power supply. An AT supply is on when the supply is connected to the AC main and the power switch that is in series with the AC main input is on. AT supplies are extinct in the commercial PC market, but the term lives on as a reference to a power supply that does not allow software control.

An ATX supply may be converted to AT style operation by simply holding the ATX PS_ON# input low all the time.

4.3 COM Express ATX and AT Power state (Refer PICMG Carrier DG Rev 2.0)

Table 4-2: COM Express Power state

State	Description	Comment
G3	Mechanical Off	System power consumption is near zero – the only power consumption is that of the RTC circuits, which are powered by a backup battery.
S5	Soft Off	System is off except for a small subset that is powered by the 5V Suspend rail.
S4	Suspend to Disk	System is off except for a small subset that is powered by the 5V Suspend rail. (that is powered off).
S3	Suspend to RAM	System is off except for system subset that includes the RAM. Suspend power is provided by the 5V Suspend rail.
S0	On	System is on.

Table 4-3: COM Express Signals SUS_S5#, SUS_S4# and SUS_S3# Power States

State	SUS_S5#	SUS_S4#	SUS_S3#
G3	NA	NA	NA
S5	Low	Low	Low
S4	High	Low	Low
S3	High	High	Low
S0	High	High	High

4.4 COM Express ATX and AT Power Sequence

A sequence diagram for an ATX style boot from a soft-off state (S5), initiated by a power button press, is shown in Figure 64 below. A sequence diagram for an AT style boot from the mechanical off state (G3) is shown in Figure 65 below.

In both cases, the VCC_12V, VCC_5V and VCC_3V3 power lines should rise together in a monotonic ramp with a positive slope only, and their rise time should be limited. Please refer to the ATX specification for more details. (Refer PICMG Carrier DG Rev 2.0)

Figure 4-2 ATX Sequence

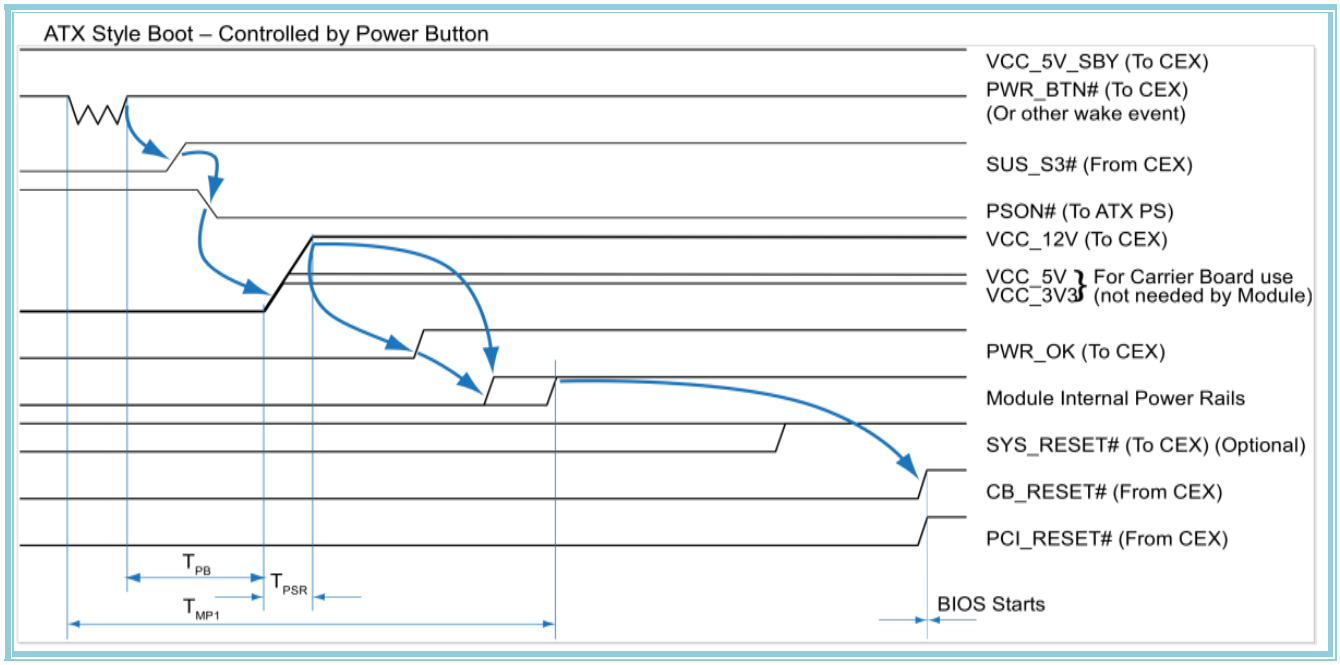


Figure 4-3 AT Sequence

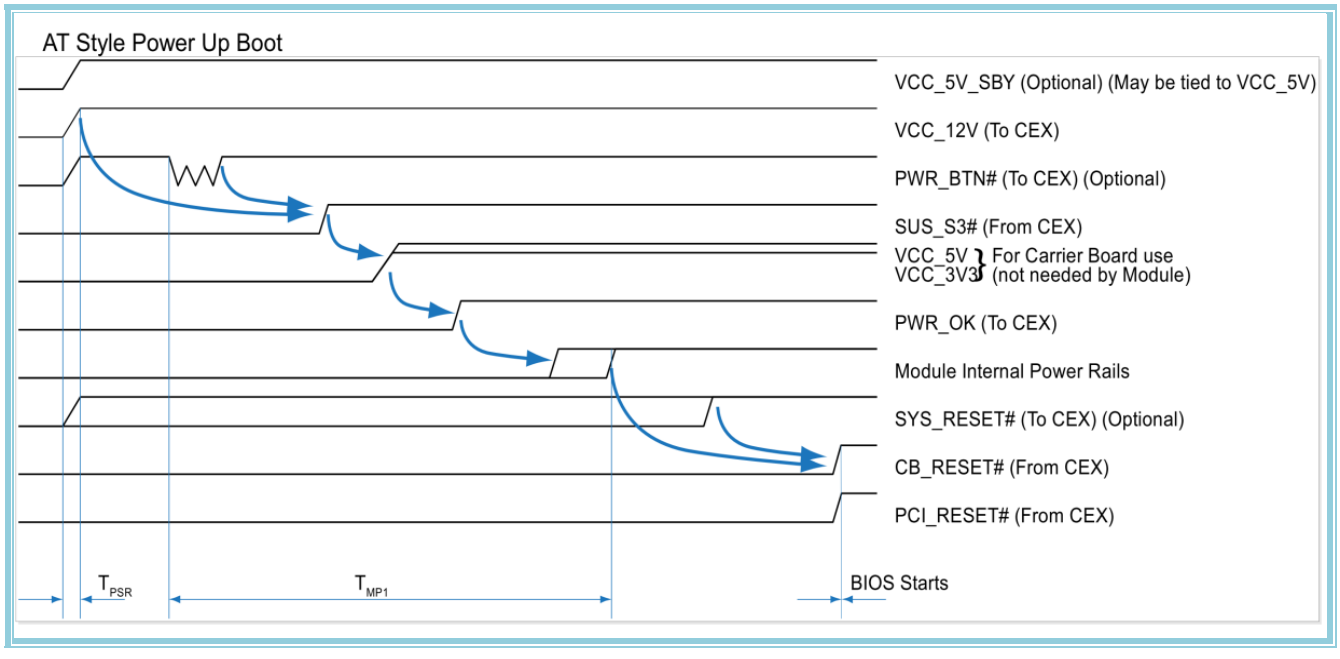
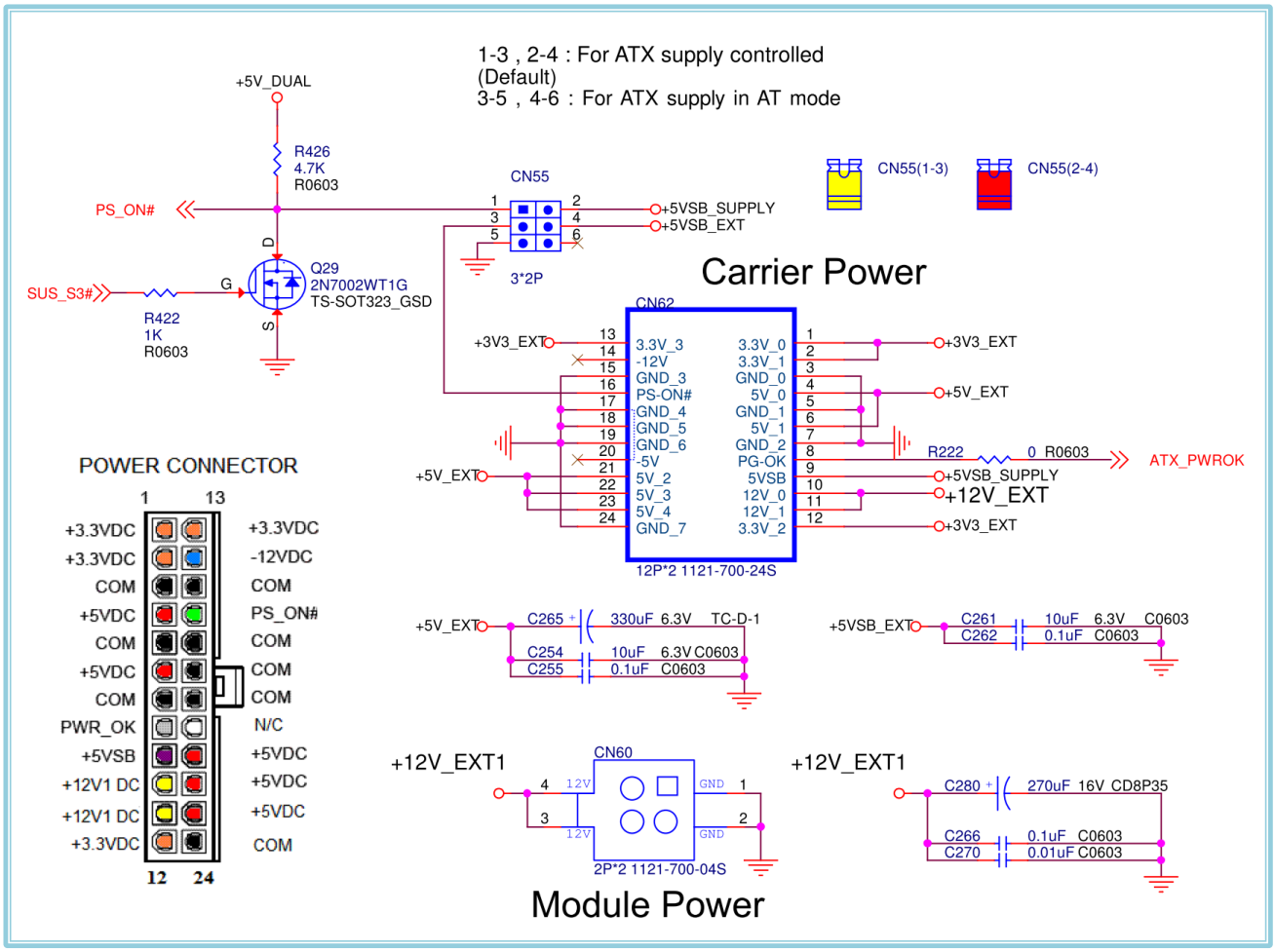


Table 4-4: ATX and AT Power Up Timing Values

Parameter	Min Value	Max Value	Description	Comments
TPB	10ms	500ms	Push Button Power Switch – time to bring Module chipset out of Suspend mode	Applies only to ATX Style Power Up
TPSR	0.1ms	20ms	Power Supply Rise Time	

4.5 Reference Schematics

Figure 4-4 COM Express Main Power



Note : Independent Power Input Design of COM Express Module Power Consumption Measurement Use.

5. **Appendix**

5.1 List of Figures

5.2 List of Tables